

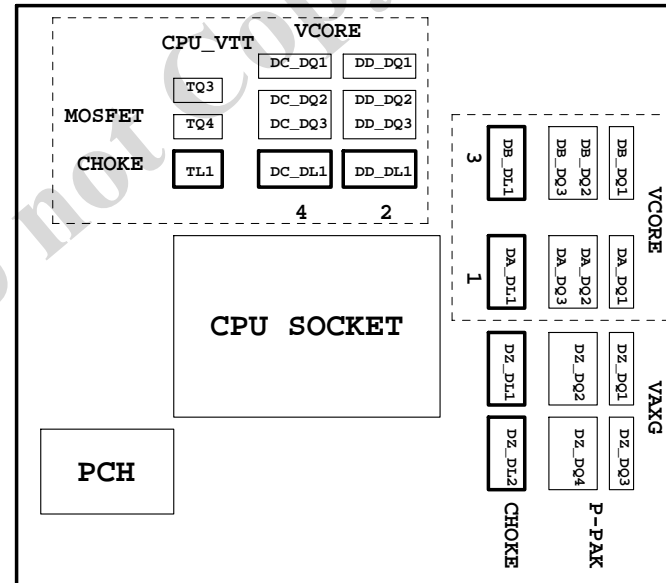
Model Name: GA-Z77-D3H

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	

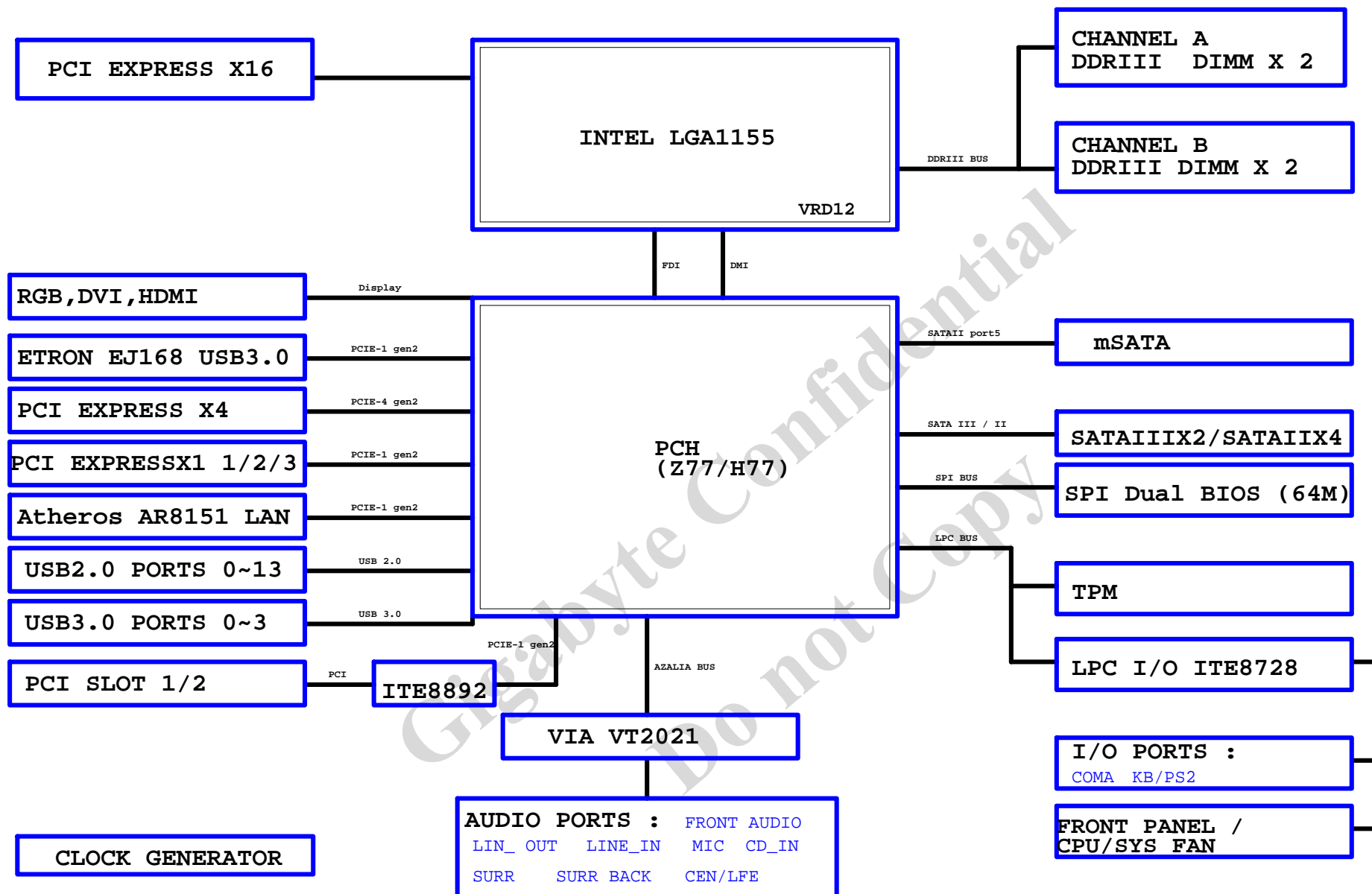


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Cover Sheet			
Title	GA-Z77-D3H		
Size	Document Number	Rev	1.0
Custom			
Date:	Monday, January 09, 2012	Sheet	1 of 38

BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990





LGA1155A

M_AAA0	AV27	SA_MA[0]	SA_DQ[0]	AK3	M_DQSA0
M_AAA1	AY24	SA_MA[1]	SA_DQ[1]	AK2	M_DQSA0
M_AAA2	AW24	SA_MA[2]			
M_AAA3	AW23	SA_MA[3]			
M_AAA4	AV23	SA_MA[4]	SA_DQ[0]	AJ3	M_DA0
M_AAA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	M_DA1
M_AAA6	AT23	SA_MA[6]	SA_DQ[2]	AL3	M_DA2
M_AAA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	M_DA3
M_AAA8	AV22	SA_MA[8]	SA_DQ[4]	AJ2	M_DA4
M_AAA9	AT22	SA_MA[9]	SA_DQ[5]	AJ1	M_DA5
M_AAA10	AV28	SA_MA[10]	SA_DQ[6]	AL2	M_DA6
M_AAA11	AU21	SA_MA[11]	SA_DQ[7]	AL1	M_DA7
M_AAA12	AT21	SA_MA[12]			
M_AAA13	AW32	SA_MA[13]	SA_DQ[11]	AP3	M_DQSA1
M_AAA14	AU20	SA_MA[14]	SA_DQ[11]	AP2	M_DQSA1
M_AAA15	AT20	SA_MA[15]			

[7] M_SWEA	M_SCASA	AV29	SA_WE#	AN1	M_DA8
[7] M_SCASA	M_SRASA	AV30	SA_CAS#	AN4	M_DA9
[7] M_SRASA		AU28	SA_RAS#	AR3	M_DA10

[7] M_SBA0	M_SBA0	AV29	SA_BS[0]	AR4	M_DA12
[7] M_SBA1	M_SBA1	AW28	SA_BS[1]	AN2	M_DA13
[7] M_SBA2	M_SBA2	AV20	SA_BS[2]	AR2	M_DA14
				AR1	M_DA15

[7] M-CSA0	M-CSA0	AV29	SA_CS#0	AW4	M_DQSA2
[7] M-CSA1	M-CSA1	AV32	SA_CS#1	AW4	M_DQSA2
[7] M-CSA2	M-CSA2	AW30	SA_CS#2		
[7] M-CSA3	M-CSA3	AU33	SA_CS#3		

[7] M_CKEA0	M_CKEA0	AV19	SA_CKE[0]	AV2	M_DA16
[7] M_CKEA1	M_CKEA1	AT19	SA_CKE[1]	AW3	M_DA17
[7] M_CKEA2	M_CKEA2	AU18	SA_CKE[2]	AV5	M_DA18
[7] M_CKEA3	M_CKEA3	AV18	SA_CKE[3]	AW5	M_DA19
				AU2	M_DA20

M_ODT_A0	AV31	SA_ODT[0]		AL3	M_DA21
M_ODT_A1	AU32	SA_ODT[1]		AU5	M_DA22
M_ODT_A2	AU30	SA_ODT[2]		AY5	M_DA23
M_ODT_A3	AW33	SA_ODT[3]			

[7] M_DCLKA0	M_DCLKA0	AY25	SA_CK[0]	AY7	M_DA24
[7] M_DCLKA0	M_DCLKA0	AW25	SA_CK#0	AU7	M_DA25
[7] M_DCLKA1	M_DCLKA1	AU24	SA_CK[1]	AW7	M_DA26
[7] M_DCLKA1	M_DCLKA1	AU25	SA_CK#1	AU9	M_DA27
[7] M_DCLKA2	M_DCLKA2	AW27	SA_CK[2]	AY7	M_DA28
[7] M_DCLKA2	M_DCLKA2	AY27	SA_CK#2	AW7	M_DA29
[7] M_DCLKA3	M_DCLKA3	AW26	SA_CK[3]	AW9	M_DA30
[7] M_DCLKA3	M_DCLKA3	AW26	SA_CK#3	AY9	M_DA31

[7,8] M_DDR3_RST		AW18	SM_DRAMRST#		
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MBC8	0.1u4/X7R/16V/K/X			AV37	M_DQSA4
				AV36	M_DQSA4

AV13	SA_DQS[8]	AU35	M_DA32	SA_DQ[32]	AW37	M_DA33
AV12	SA_DQS[8]	AU36	M_DA34	SA_DQ[33]	AU39	M_DA34
		AU36	M_DA35	SA_DQ[34]	AU36	M_DA35
		AY36	M_DA36	SA_DQ[35]	AW35	M_DA36
AU12	SA_ECC_CB[0]	AY36	M_DA37	SA_DQ[36]	AU36	M_DA37
AU14	SA_ECC_CB[1]	AU37	M_DA38	SA_DQ[37]	AU38	M_DA38
AV13	SA_ECC_CB[2]	AU37	M_DA39	SA_DQ[38]	AU37	M_DA39
AY13	SA_ECC_CB[3]			SA_DQ[39]		
AU11	SA_ECC_CB[4]	AP38	M_DQSA5			
AY12	SA_ECC_CB[5]	AP39	M_DQSA5			
AW12	SA_ECC_CB[7]					

AR40	M_DA40	SA_DQ[40]		AK38	M_DQSA6
AR37	M_DA41	SA_DQ[41]		AK39	M_DQSA6
AN38	M_DA42	SA_DQ[42]			
AN37	M_DA43	SA_DQ[43]			
AR39	M_DA44	SA_DQ[44]			
AR38	M_DA45	SA_DQ[45]			
AN38	M_DA46	SA_DQ[46]			
AN40	M_DA47	SA_DQ[47]			

AK38	M_DQSA6	SA_DQS[6]			
AK39	M_DQSA6	SA_DQS[6]			

AL40	M_DA48	SA_DQ[48]			
AL37	M_DA49	SA_DQ[49]			
AJ38	M_DA50	SA_DQ[50]			
AJ37	M_DA51	SA_DQ[51]			
AL39	M_DA52	SA_DQ[52]			
AL38	M_DA53	SA_DQ[53]			
AJ39	M_DA54	SA_DQ[54]			
AJ40	M_DA55	SA_DQ[55]			

AF38	M_DQSA7	SA_DQS[7]			
AF39	M_DQSA7	SA_DQS[7]			

AG40	M_DA56	SA_DQ[56]			
AG37	M_DA57	SA_DQ[57]			
AE38	M_DA58	SA_DQ[58]			
AE37	M_DA59	SA_DQ[59]			
AG39	M_DA60	SA_DQ[60]			
AG38	M_DA61	SA_DQ[61]			
AE39	M_DA62	SA_DQ[62]			
AE40	M_DA63	SA_DQ[63]			

DDR_0

1 OF 10

LGA1155[10SC1-F01155-01R]

LGA1155B

M_AAB0	AK24	SB_MA[0]	SB_DQS[0]	AH7	M_DQSB0
M_AAB1	AM20	SB_MA[1]	SB_DQS[0]	AH6	M_DQSB0
M_AAB2	AM19	SB_MA[2]			
M_AAB3	AK18	SB_MA[3]			
M_AAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	M_DB0
M_AAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	M_DB1
M_AAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	M_DB2
M_AAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	M_DB3
M_AAB8	AY17	SB_MA[8]	SB_DQ[4]	AG5	M_DB5
M_AAB9	AN18	SB_MA[9]	SB_DQ[5]	AG6	M_DB6
M_AAB10	AN23	SB_MA[10]	SB_DQ[6]	AJ6	M_DB6
M_AAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	M_DB7
M_AAB12	AT18	SB_MA[12]			
M_AAB13	AR26	SB_MA[13]	SB_DQS[11]	AM8	M_DQSB1
M_AAB14	AY16	SB_MA[14]	SB_DQS[11]	AL8	M_DQSB1
M_AAB15	AV16	SB_MA[15]			

[8] M_SWEB	M_SWEB	AR25	SB_WE#	SB_DQ[8]	AL7	M_DB8
[8] M_SCASB	M_SCASB	AK25	SB_CAS#	SB_DQ[9]	AM7	M_DB9
[8] M_SRASB	M_SRASB	AP24	SB_RAS#	SB_DQ[10]	AM10	M_DB10

[8] M_SBA0	M_SBA0	AP23	SB_BS[0]	SB_DQ[11]	AL6	M_DB11
[8] M_SBA1	M_SBA1	AM22	SB_BS[1]	SB_DQ[12]	AM6	M_DB12
[8] M_SBA2	M_SBA2	AW17	SB_BS[2]	SB_DQ[13]	AL9	M_DB14
				SB_DQ[14]	AM9	M_DB15

[8] M-CSB0	M-CSB0	AN25	SB_CS#0	SB_DQS[2]	AR8	M_DQSB2
[8] M-CSB1	M-CSB1	AN26	SB_CS#1	SB_DQS[2]	AP8	M_DQSB2
[8] M-CSB2	M-CSB2	AL25	SB_CS#2			
[8] M-CSB3	M-CSB3	AT26	SB_CS#3			

[8] M_CKEB0	M_CKEB0	AU18	SB_CKE[0]	SB_DQ[16]	AP7	M_DB16
[8] M_CKEB1	M_CKEB1	AY15	SB_CKE[1]	SB_DQ[17]	AR7	M_DB17
[8] M_CKEB2	M_CKEB2	AW15	SB_CKE[2]	SB_DQ[18]	AP10	M_DB18
[8] M_CKEB3	M_CKEB3	AV15	SB_CKE[3]	SB_DQ[19]	AR10	M_DB19
				SB_DQ[20]	AP6	M_DB20

M_ODT_B0	AL26	SB_ODT[0]		AR6	M_DB21
M_ODT_B1	AP26	SB_ODT[1]		AP9	M_DB22
M_ODT_B2	AM26	SB_ODT[2]		AR9	M_DB23
M_ODT_B3	AK26	SB_ODT[3]			

[8] M_DCLKB0	M_DCLKB0	AL21	SB_CK[0]	SB_DQS[3]	AN13	M_DQSB3
[8] M_DCLKB0	M_DCLKB0	AL22	SB_CK#0	SB_DQS[3]	AN12	M_DQSB3
[8] M_DCLKB1	M_DCLKB1	AL20	SB_CK[1]			
[8] M_DCLKB1	M_DCLKB1	AK20	SB_CK#1	SB_DQ[24]	AM12	M_DB24
[8] M_DCLKB2	M_DCLKB2	AL23	SB_CK[2]	SB_DQ[25]	AM13	M_DB25
[8] M_DCLKB2	M_DCLKB2	AM22	SB_CK#2	SB_DQ[26]	AR13	M_DB26
[8] M_DCLKB3	M_DCLKB3	AP21	SB_CK[3]	SB_DQ[27]	AP13	M_DB27
[8] M_DCLKB3	M_DCLKB3	AN21	SB_CK#3	SB_DQ[28]	AL12	M_DB28
				SB_DQ[29]	AL13	M_DB29
				SB_DQ[30]	AR12	M_DB30
				SB_DQ[31]	AP12	M_DB31

[8] M_VREF_DQB		AH1	FC_AH1	SB_DQS[4]	AN29	M_DQSB4
[7] M_VREF_DOA		AH4	FC_AH4	SB_DQS[4]	AN28	M_DQSB4

AN16	SB_DQS[8]	SB_DQ[32]	AR28	M_DB32
AN15	SB_DQS[8]	SB_DQ[33]	AL28	M_DB34
		SB_DQ[34]	AL29	M_DB35
		SB_DQ[35]	AP28	M_DB36
		SB_DQ[36]	AP28	M_DB37
		SB_DQ[37]	AM28	M_DB38
		SB_DQ[38]	AM29	M_DB39
		SB_DQ[39]		

AN16	SB_DQS[8]	SB_DQS[5]	AP33	M_DQSB5
AN15	SB_DQS[8]	SB_DQS[5]	AR33	M_DQSB5

AL16	SB_ECC_CB[0]	SB_DQ[40]	AP21	M_DB40
AM16	SB_ECC_CB[1]	SB_DQ[41]	AP35	M_DB42
AP16	SB_ECC_CB[2]	SB_DQ[42]	AP34	M_DB43
AR16	SB_ECC_CB[3]	SB_DQ[43]	AP32	M_DB44
AL15	SB_ECC_CB[4]	SB_DQ[44]	AR31	M_DB45
AM15	SB_ECC_CB[5]	SB_DQ[45]	AR35	M_DB46
AP15	SB_ECC_CB[6]	SB_DQ[46]	AR34	M_DB47
		SB_DQ[47]		

AL16	SB_ECC_CB[0]	SB_DQS[6]	AL33	M_DQSB6
AM16	SB_ECC_CB[1]	SB_DQS[6]	AM33	M_DQSB6

AP16	SB_ECC_CB[2]	SB_DQ[48]	AM32	M_DB48
AR16	SB_ECC_CB[3]	SB_DQ[49]	AM31	M_DB49
AL15	SB_ECC_CB[4]	SB_DQ[50]	AL35	M_DB50
AM15	SB_ECC_CB[5]	SB_DQ[51]	AL32	M_DB51
AP15	SB_ECC_CB[6]	SB_DQ[52]	AM34	M_DB52
		SB_DQ[53]	AL31	M_DB53
		SB_DQ[54]	AM35	M_DB54
		SB_DQ[55]	AL34	M_DB55

AG35	M_DQSB7	SB_DQS[7]			
AG34	M_DQSB7	SB_DQS[7]			

AH35	M_DB56	SB_DQ[56]			
AH34	M_DB57	SB_DQ[57]			
AE34	M_DB58	SB_DQ[58]			
AE35	M_DB59	SB_DQ[59]			
AJ35	M_DB60	SB_DQ[60]			
AJ34	M_DB61	SB_DQ[61]			
AE33	M_DB62	SB_DQ[62]			
AF33	M_DB63	SB_DQ[63]			

AL33	M_DQSB6	SB_DQS[6]			
AM33	M_DQSB6	SB_DQS[6]			

AM32	M_DB48	SB_DQ[48]			
AM31	M_DB49	SB_DQ[49]			
AL35	M_DB50	SB_DQ[50]			
AL32	M_DB51	SB_DQ[51]			
AM34	M_DB52	SB_DQ[52]			
AL31	M_DB53	SB_DQ[53]			
AM35	M_DB54	SB_DQ[54]			
AL34	M_DB55	SB_DQ[55]			

AG35	M_DQSB7	SB_DQS[7]			
AG34	M_DQSB7	SB_DQS[7]			

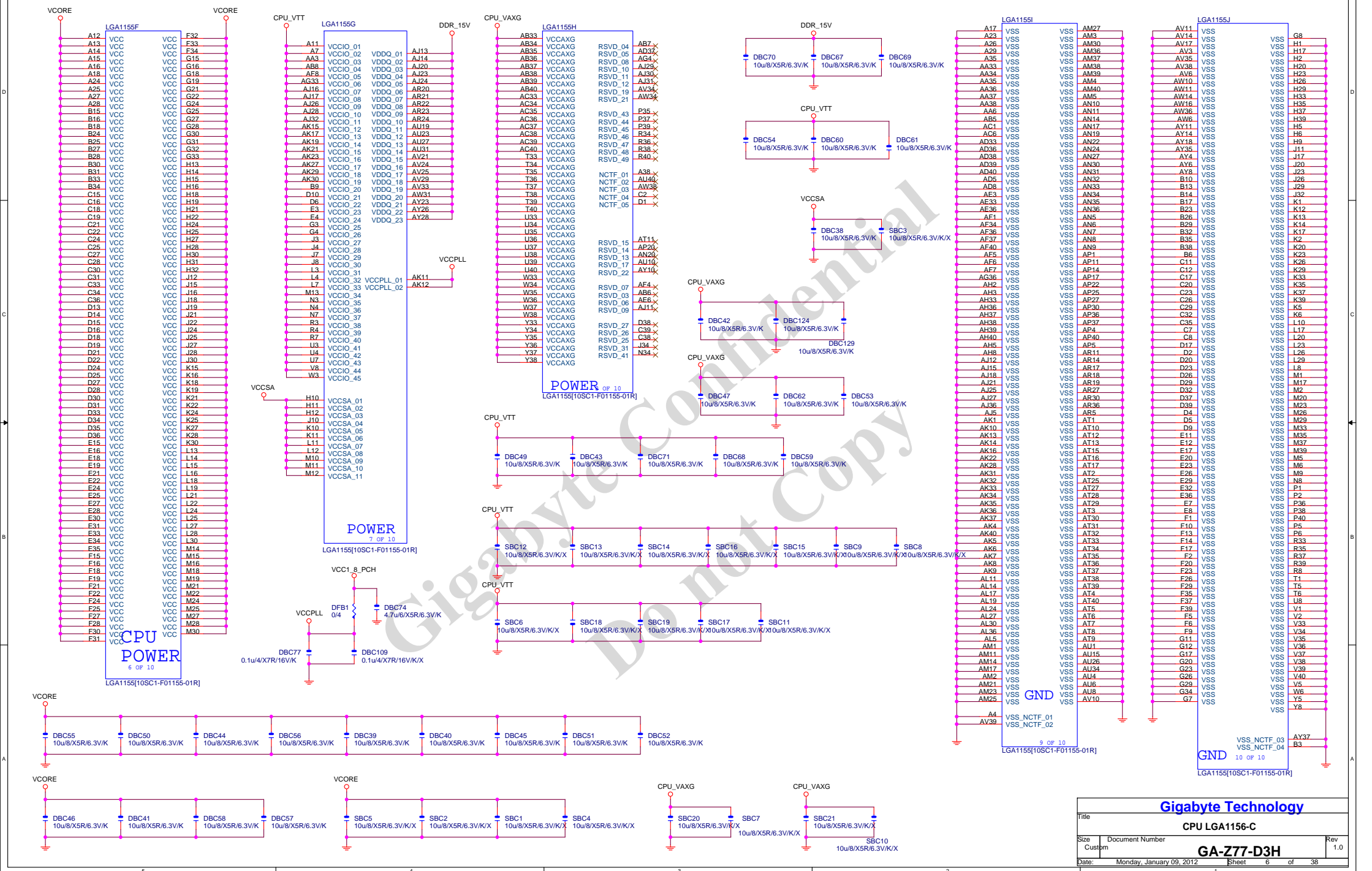
AH35	M_DB56	SB_DQ[56]			
AH34	M_DB57	SB_DQ[57]			
AE34	M_DB58	SB_DQ[58]			
AE35	M_DB59	SB_DQ[59]			
AJ35	M_DB60	SB_DQ[60]			
AJ34	M_DB61	SB_DQ[61]			
AE33	M_DB62	SB_DQ[62]			
AF33	M_DB63	SB_DQ[63]			

AG35	M_DQSB7	SB_DQS[7]			
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AH35	M_DB56	SB_DQ[56]			
AH34	M_DB57	SB_DQ[57]			
AE34	M_DB58	SB_DQ[58]			
AE35	M_DB59	SB_DQ[59]			
AJ35	M_DB60	SB_DQ[60]			
AJ34	M_DB61	SB_DQ[61]			
AE33	M_DB62	SB_DQ[62]			
AF33	M_DB63	SB_DQ[63]			

AG35	M_DQSB7	SB_DQS[7]			
AG34	M_DQSB7	SB_DQS[7]			

SB_DQ[60]	AJ35	M	DB60
SB_DQ[61]	AJ34	M	DB61
SB_DQ[62]	AF33	M	DB62
SB_DQ[63]	AF35	M	DB63



Gigabyte Technology

CPU LGA1156-C

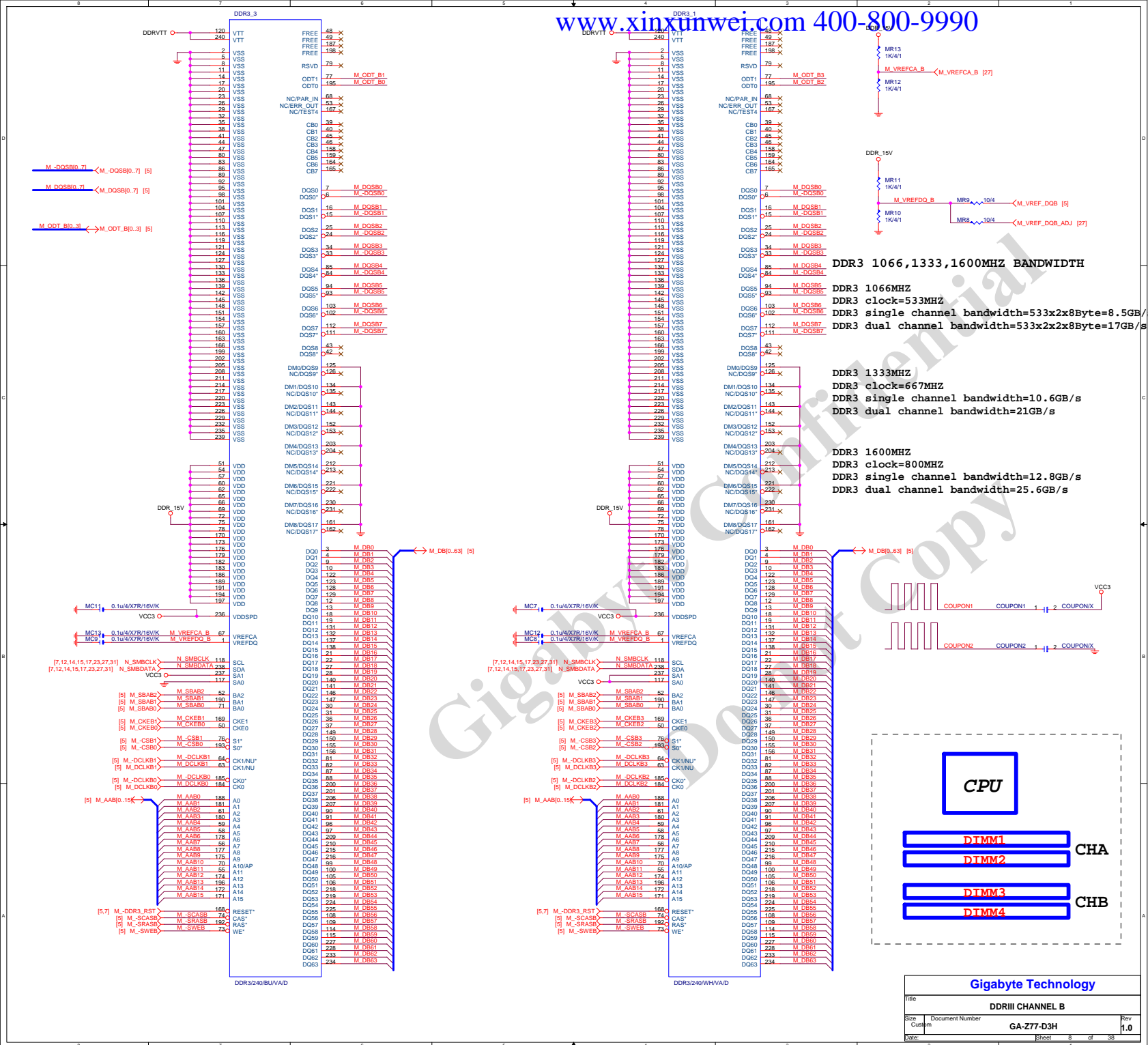
Title	Document Number	Rev
Size	Custom	1.0
Date	Monday, January 09, 2012	Sheet 6 of 38

GA-Z77-D3H

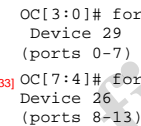


DDR 15V

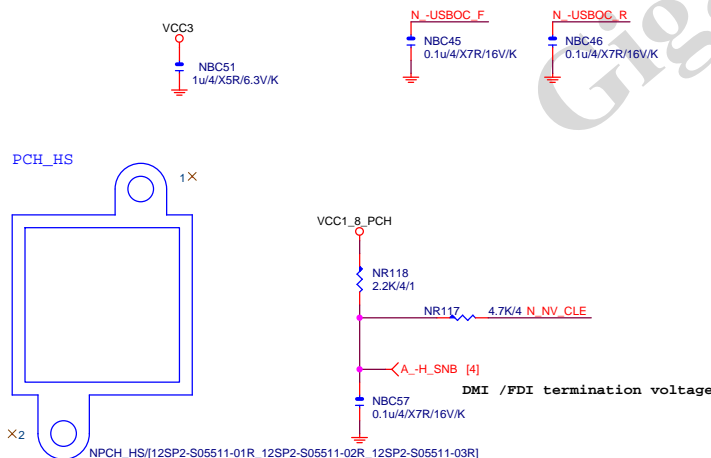
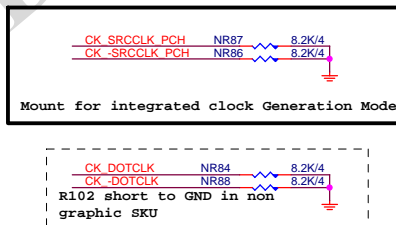
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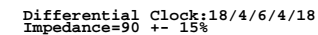
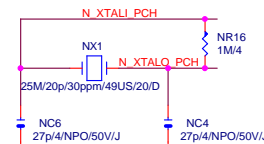


Impedance=85 +/- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

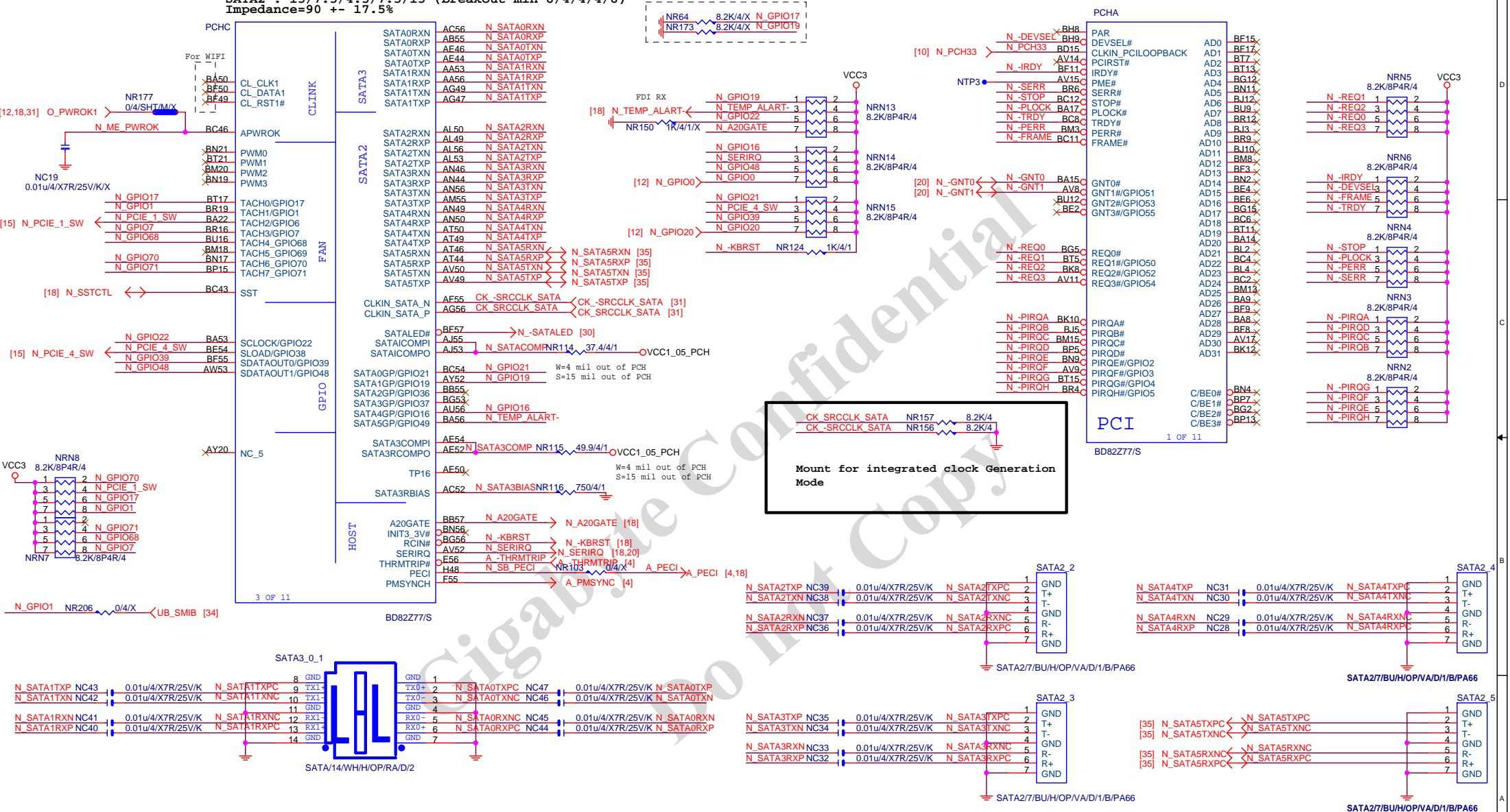


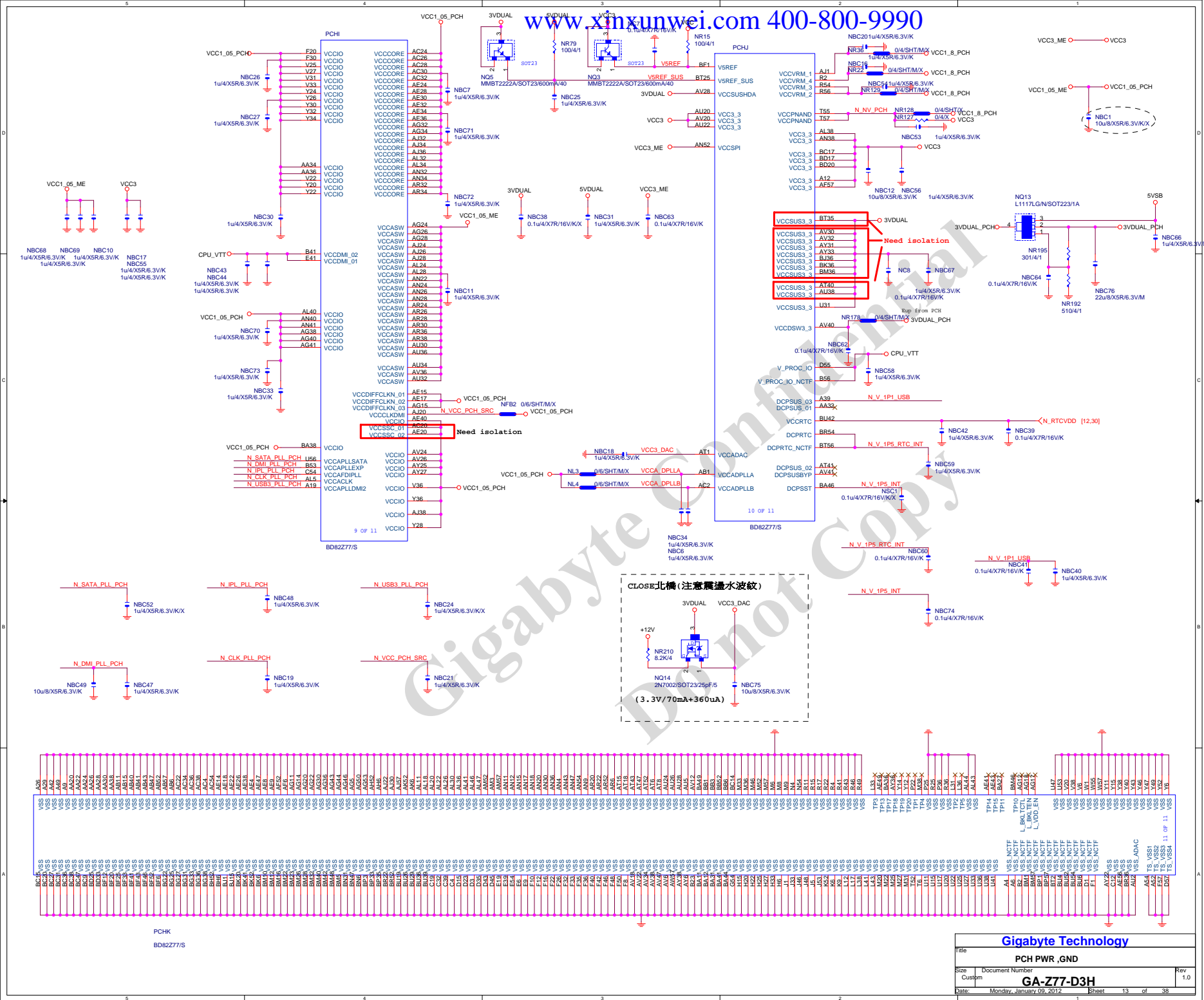
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OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use





SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

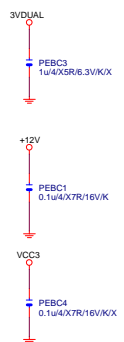
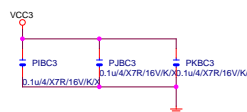
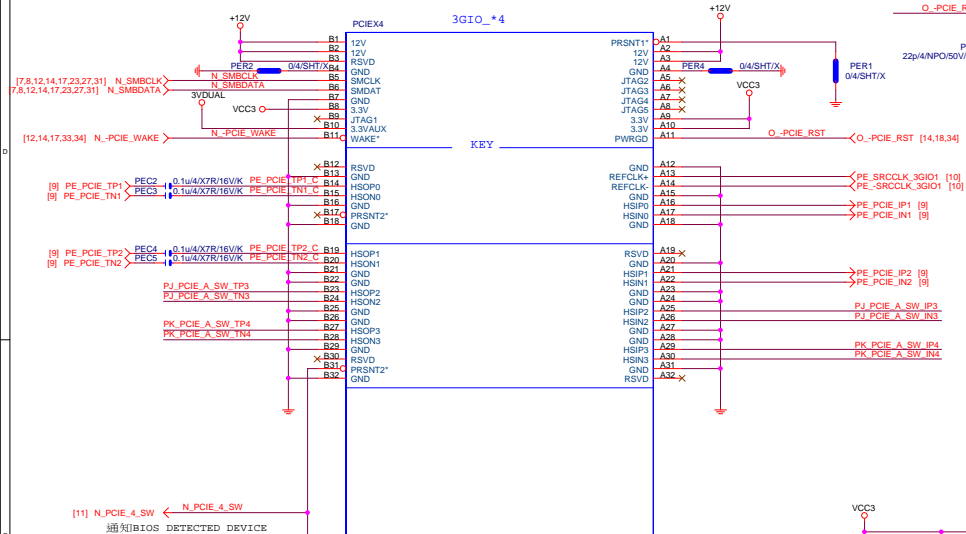






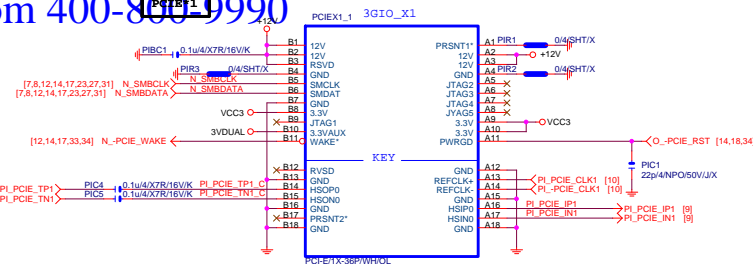
PCI-E REV:2.0--> 5GHZ

PCIE*4

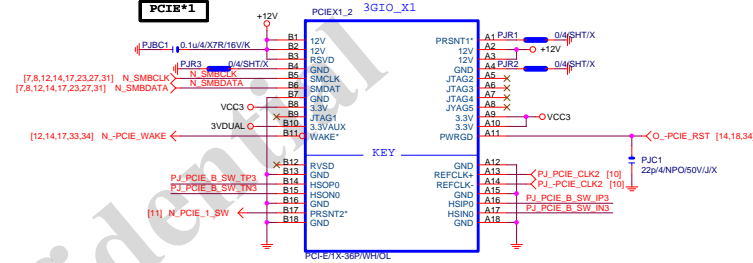


	N_PCIE_4_SW (PCH GPIO38)	PCIE_X1_1 (SIO_GPIO26)
PCIE_X1, PCIE_X4 --> X1 (Default)	H	H
PCIE_X1_2/PCIE_X1_3 Have devices PCIE_X4 --> X1	H	H
PCIE_X1_2/PCIE_X1_3 No devices PCIE_X4 Have devices PCIE_X4 --> X4	L	L

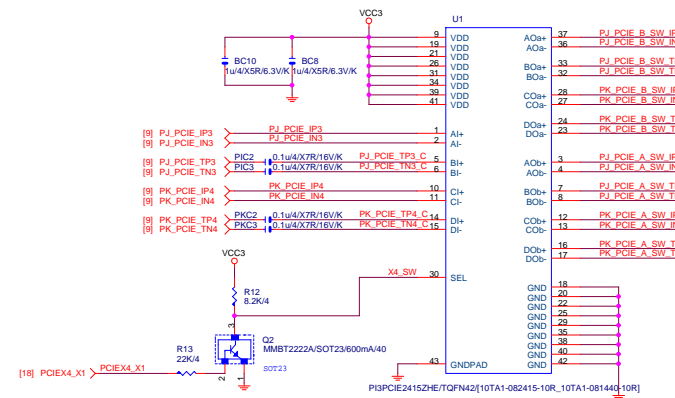
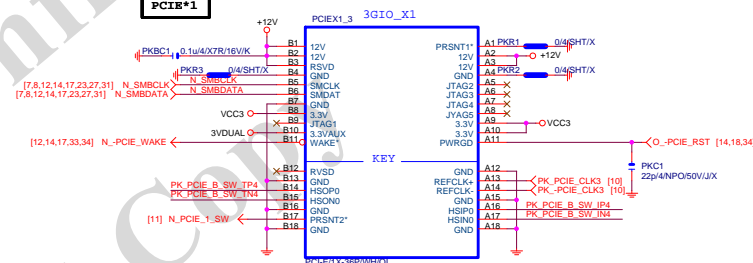
PCIE*1



PCIE*1



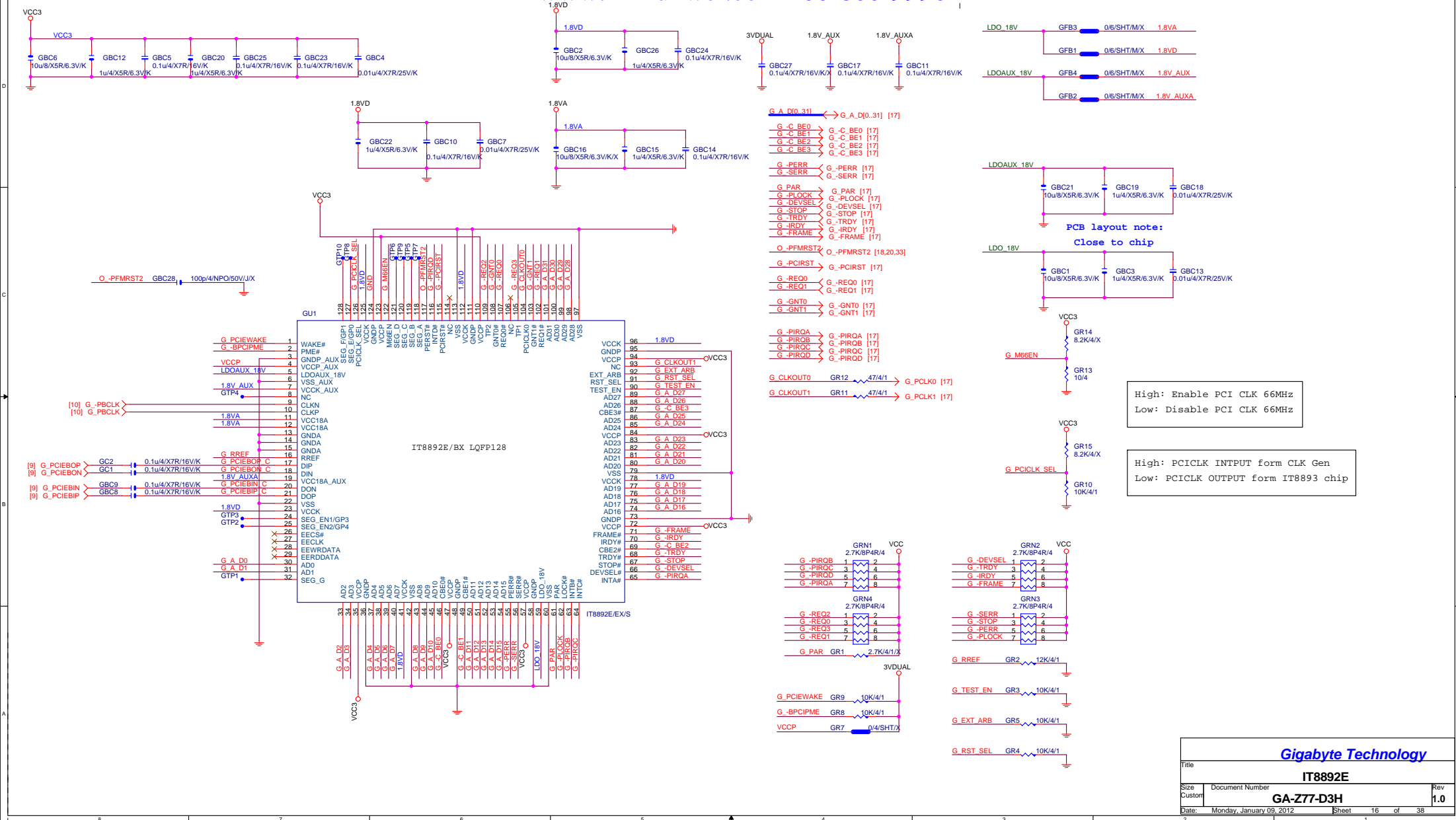
PCIE*1



Function	SEL
X1--> x0a	L ₁ PCIE_X4 SLOT-->X1
X1--> x0b	H ₁ PCIE_X4 SLOT-->X4

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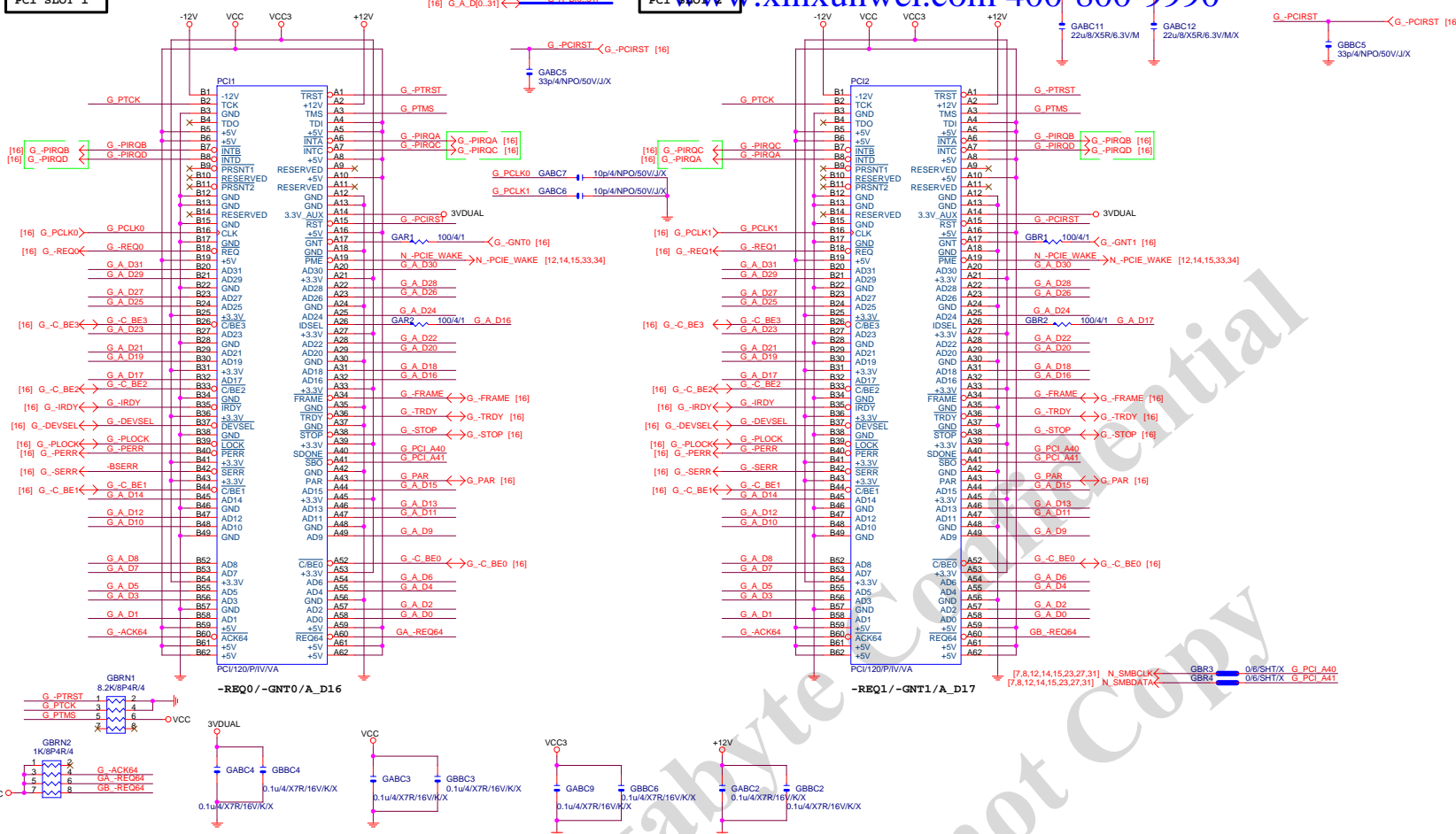
PCIE X1 1.2		
Title	Document Number	Rev
Size	Custom	1.0
Date	Monday, January 09, 2012	Printed 15 of 38



PCI SLOT 1

PCI SLOT 2

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GIGABYTE™			
Title PCI SLOT 1&2			
Size	Document Number		Rev
Custom	GA-Z77-D3H		1.0
Date: Monday, January 09, 2012		Sheet 17 of 38	

www.xinxunwei.com 400-800-9990

IT8728F(GB)

Pinout Table:

PIN	ITE8721	ITE8728
PIN121	FAN_CTL4 / VID_TURBO	VCORE_EN / PCH_C0
PIN120	VDDA_EN	VLDT_EN / PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST / AMDTSI_D / PECI_AVA / MTRB# / PCH_D	SST / AMDTSI_D / MTRB# / PCH_D1
PIN55	PECI / AMDTSI_C / DRVVB# / PCH_C	PECI / AMDTSI_C / DRVVB#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3 / ATXPG	VIN2 (VCC5)
PIN96	VIN2	VINI (VCC12)
PIN97	VINI (VCC5)	VINI / VDIMM_STR (1.5V)
PIN98	VINO (VCC12)	VINO / VCORE (1.1V)

Gigabyte Technology

ITE 8728 LPC IO

GA-Z77-D3H

Rev 1.0

Date: Monday, January 09, 2012 **Sheet** 18 **of** 38

www.xinxunwei.com 400-800-9990

IT8728F(GB)

Pinout Table:

PIN	ITE8721	ITE8728
PIN121	FAN_CTL4 / VID_TURBO	VCORE_EN / PCH_C0
PIN120	VDDA_EN	VLDT_EN / PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST / AMDTSI_D / PECI_AVA / MTRB# / PCH_D	SST / AMDTSI_D / MTRB# / PCH_D1
PIN55	PECI / AMDTSI_C / DRVVB# / PCH_C	PECI / AMDTSI_C / DRVVB#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3 / ATXPG	VIN2 (VCC5)
PIN96	VIN2	VINI (VCC12)
PIN97	VINI (VCC5)	VINI / VDIMM_STR (1.5V)
PIN98	VINO (VCC12)	VINO / VCORE (1.1V)

Gigabyte Technology

ITE 8728 LPC IO

GA-Z77-D3H

Rev 1.0

Date: Monday, January 09, 2012 **Sheet** 18 **of** 38

www.xinxunwei.com 400-800-9990

IT8728F (GB)

IT8728/EX (GB)/QFP128

IT8721

IT8728

PIN	IT8721	IT8728
PIN121	FAN_CTL4 / VID_TURBO	VCORE_EN / PCH_C0
PIN120	VDDA_EN	VLDT_EN / PCH_D0
PIN119	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST / AMDTSI_D / PECI_AVA / MTRB# / PCH_D	SST / AMDTSI_D / MTRB# / PCH_D1
PIN55	PECI / AMDTSI_C / DRV# / PCH_C	PECI / AMDTSI_C / DRV#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3 / ATXPG	VIN2 (VCC5)
PIN96	VIN2	VIN1 (VCC12)
PIN97	VIN1 (VCC5)	VIN1 / VDIMM_STR (1.5V)
PIN98	VIN0 (VCC12)	VIN0 / VCORE (1.1V)

Hi : Disable WDT
Lo : Enable WDT to rest PWROK

Gigabyte Technology

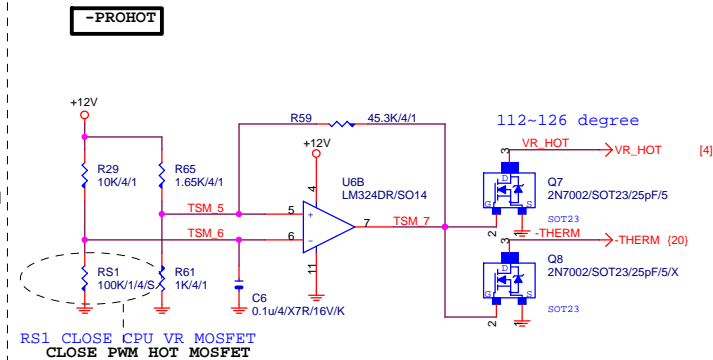
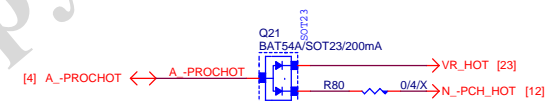
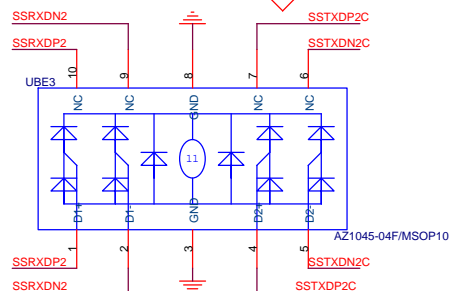
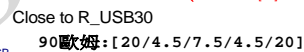
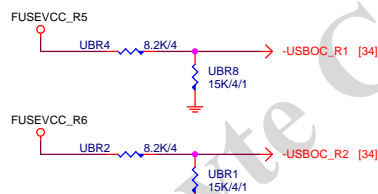
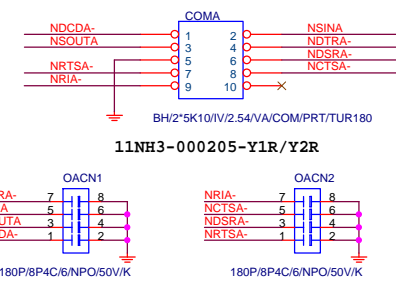
ITE 8728 LPC IO

GA-Z77-D3H

Rev 1.0

Date: Monday, January 09, 2012

Sheet 18 of 38



[12] N_ICH_SPI_MOSI >> N_ICH_SPI_MOSI NR10 8.2K/4/X
 [12] N_-ICH_SPI_CS >> N_-ICH_SPI_CS NR9 8.2K/4/X
 -SPI_HOLD0 NR3 1K/4/1
 -SPI_HOLD1 NR11 1K/4/1

[12] N_-SPI_WP1 >> N_-SPI_WP1 NR2 8.2K/4/X
 [12] N_-SPI_WP0 >> N_-SPI_WP0 NR1 8.2K/4/X
 [12] N_ICH_SPI_MISO >> N_ICH_SPI_MISO NR5 8.2K/4

[11] N_-GNT0 >> NR26 1K/4/1/X
 [11] N_-GNT1 >> NR25 1K/4/1/X

Default int pull up

SPI_MISO NR6 22/4 <<< N_ICH_SPI_MISO [12]

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

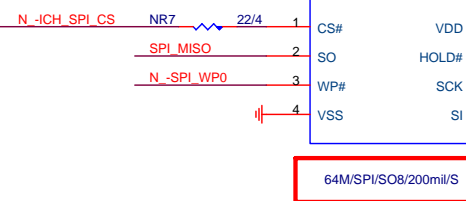
1 means floating
 0 means PD 1K

Gigabyte Technology

Title	BIOS		
Size	Document Number	GA-Z77-D3H	
Custom		Rev	1.0
Date:	Monday, January 09, 2012	Sheet	20 of 38

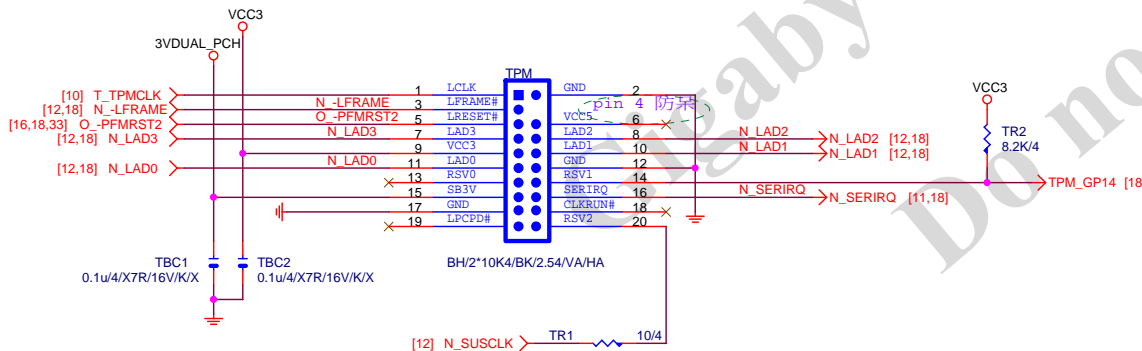
VCC3
 NBC4
 0.1u/4/X7R/16V/K

NC1
 10p/4/NPO/50V/J/X



-SPI_HOLD0 <<< -SPI_HOLD0 [18]

NC2
 10p/4/NPO/50V/J/X



VCC3
 TR2
 8.2K/4

N_SERIRQ >> N_SERIRQ [11,18]

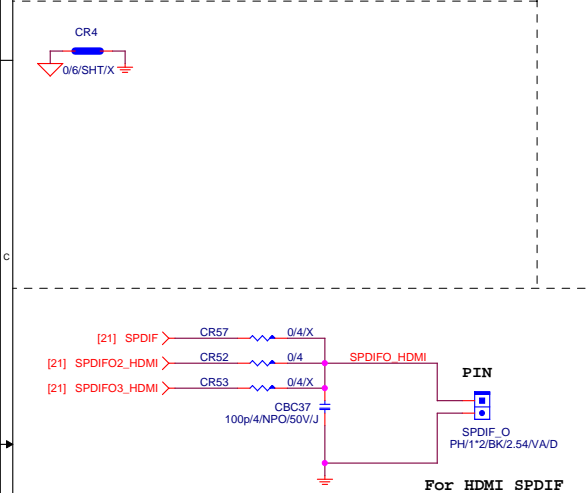
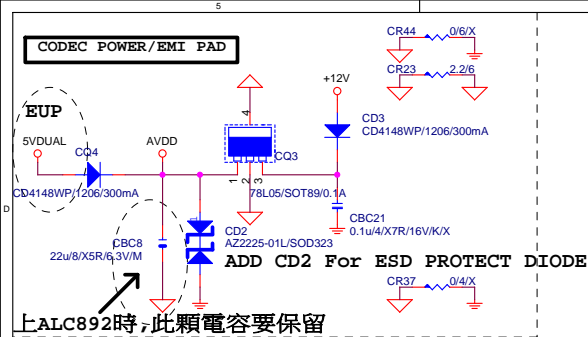
TPM_GP14 [18]

[12] N_SUSCLK >> TR1 10/4


```
CR36: 20K/4/1% @Realtek cdec & VT1708S-CE
CR36: 5.1K/4/1 @VIA codec VT1708S-CD/VT2021
CBC38 100P @VIA codec VT1708S
```

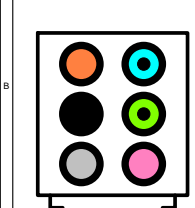


Title				HD AUDIO VT2021			
Size Custom		Document Number				Rev	
		GA-Z77-D3H				1.0	
Date:		Monday, January 09, 2012		Sheet		21 of 38	

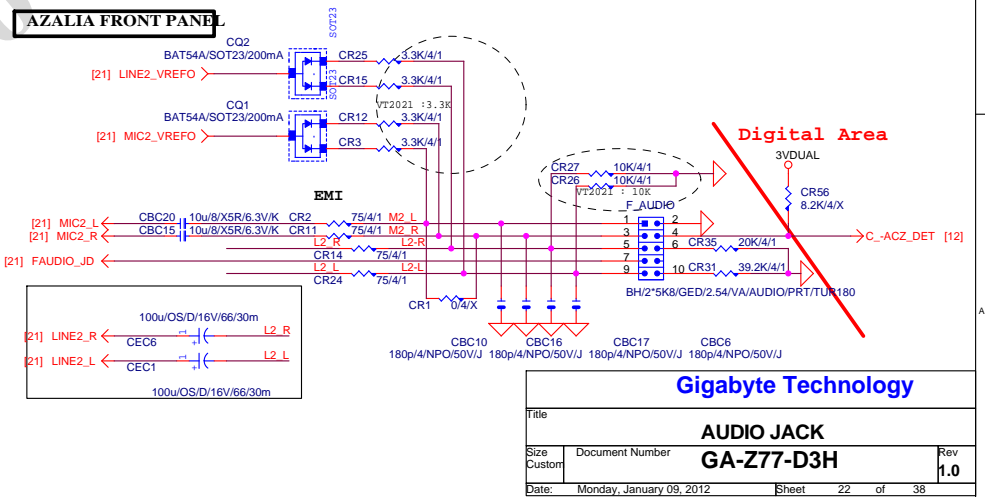
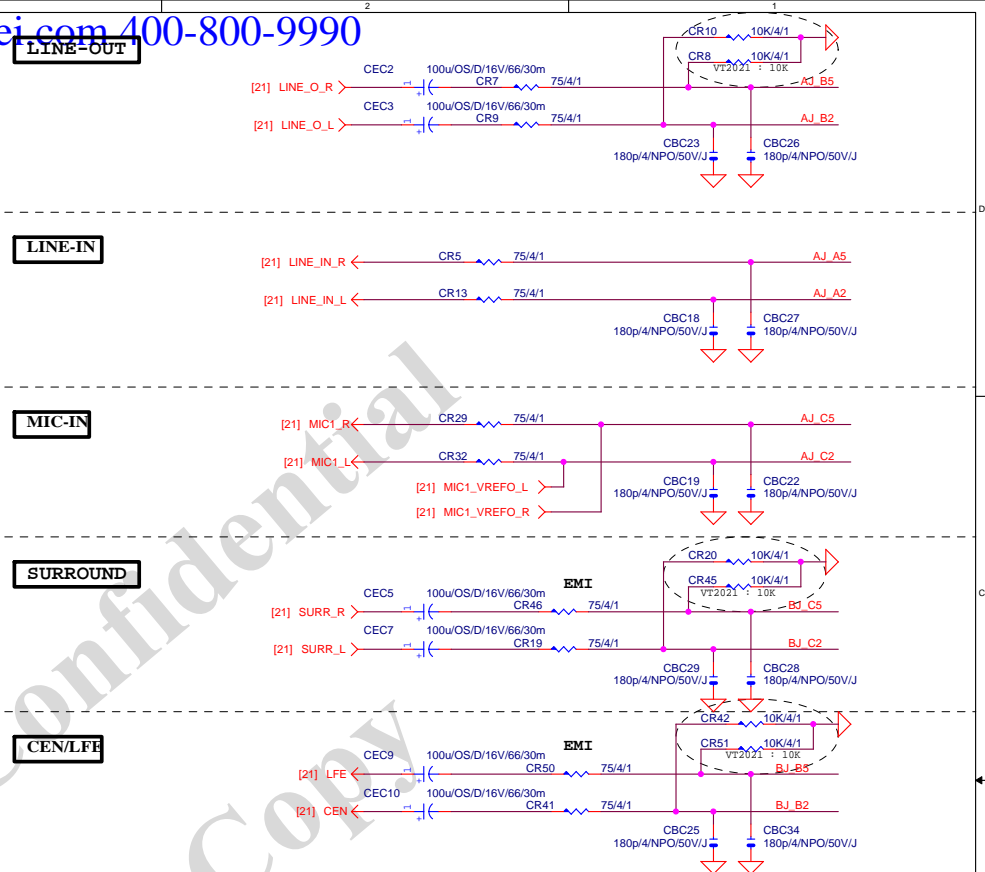
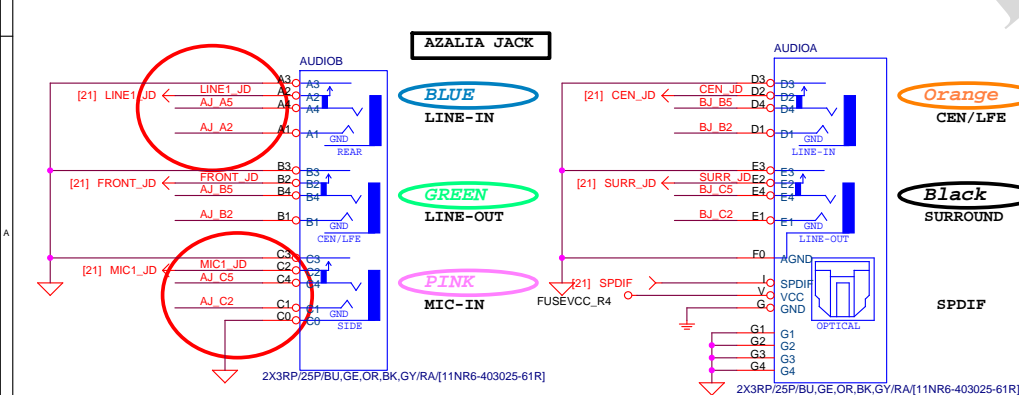


AZALIA JACK

BTX AZALIA CONNECTOR



11NR6-403007-21R

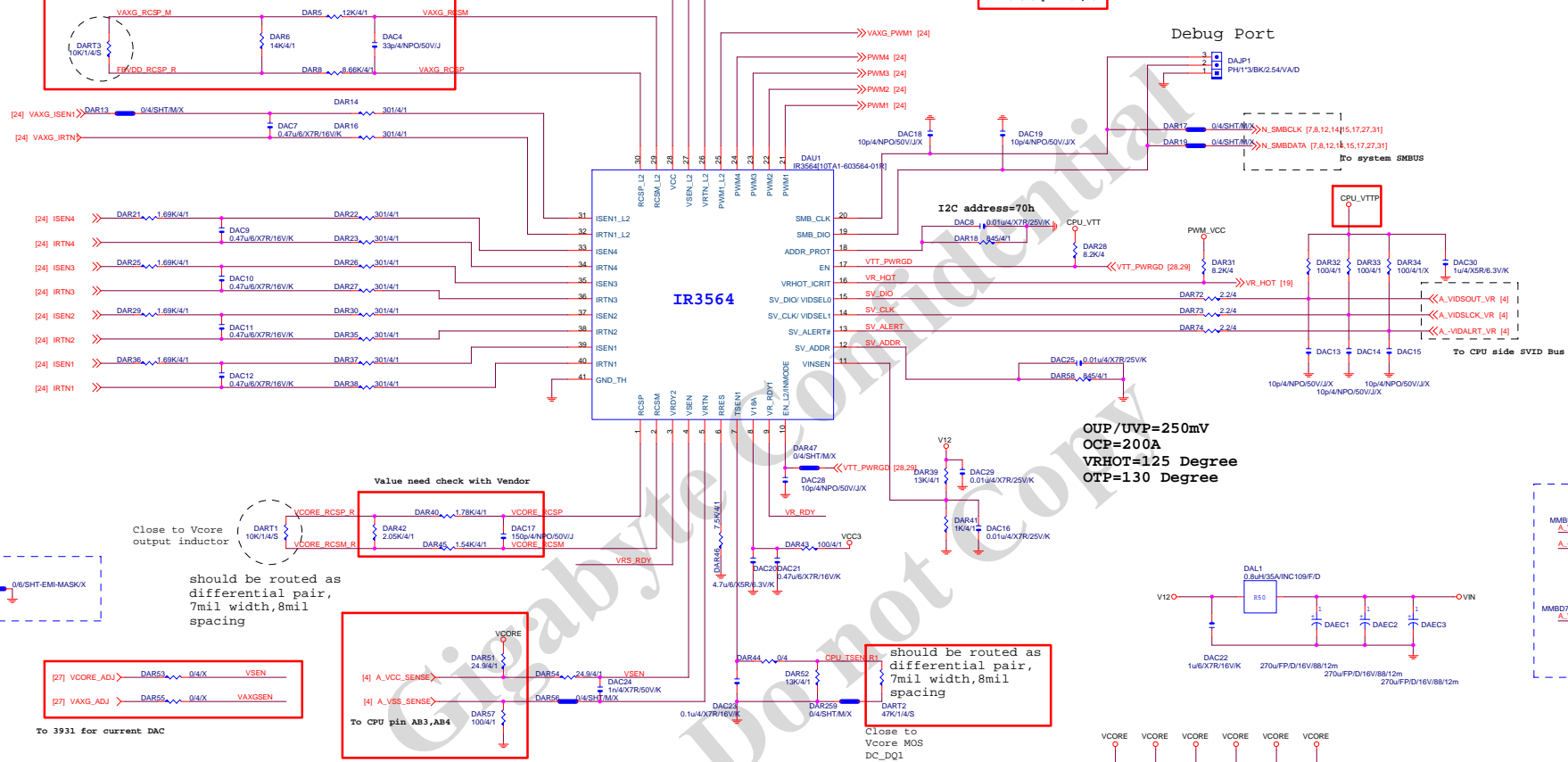


need 0.1Amp, check trace width

Value need check with Vendor

Close to VSA
output inductor

should be routed as
differential pair,
7mil width, 8mil
spacing



OUP/UVF=250mV
OCP=200A
VRHOT=125 Degree
OTP=130 Degree

Close to Vcore
output inductor

should be routed as
differential pair,
7mil width, 8mil
spacing

To 3931 for current DAC

[27] Vcore_ADJ >> DAR53 >> 0.4/X >> VSEN

[27] VAXG_ADJ >> DAR55 >> 0.4/X >> VAXGSEN

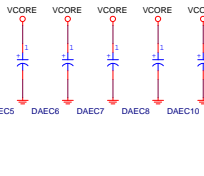
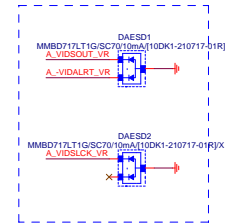
Value need check with Vendor

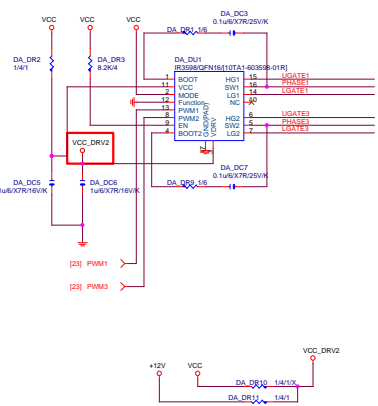
Close to Vcore
output inductor

should be routed as
differential pair,
7mil width, 8mil
spacing

should be routed as
differential pair,
7mil width, 8mil
spacing

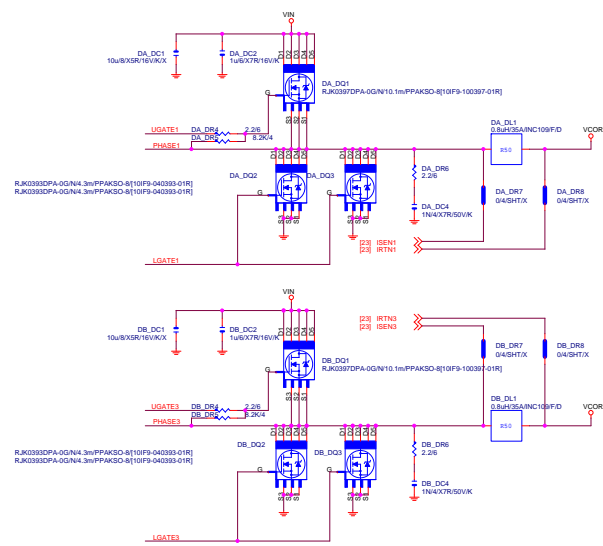
Close to Vcore MOS
DC_DQ1



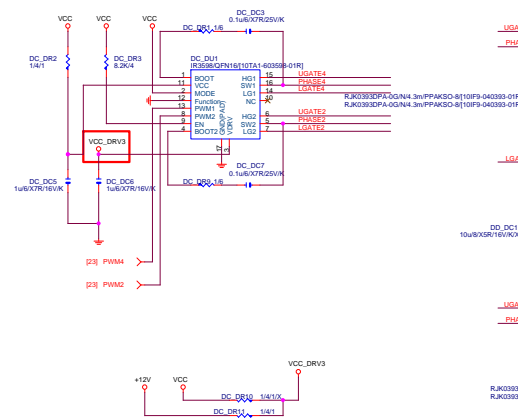
VCORE Phase
1,3

FUNCTION	MODE	PER MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IR ATL	Quad

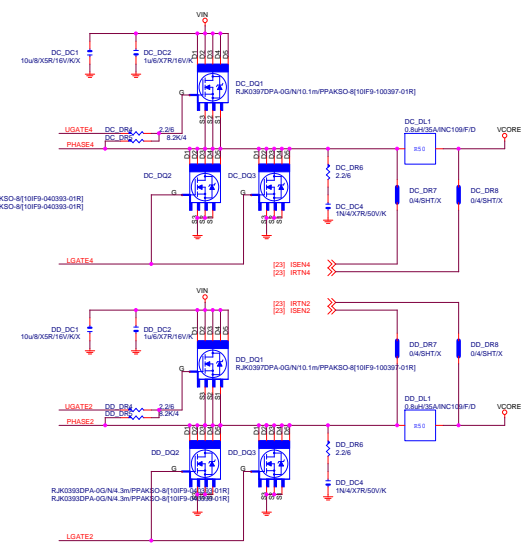
In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU



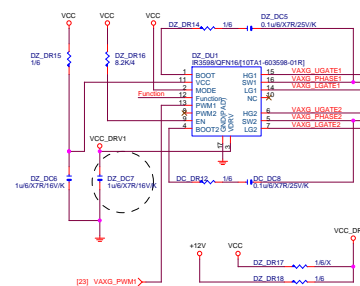
VCORE Phase 4,2



VAXG Phase



VAXG PHASE 1,2



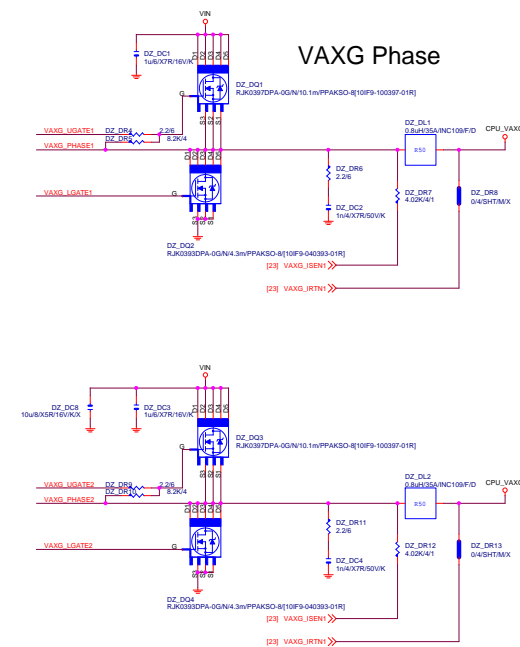
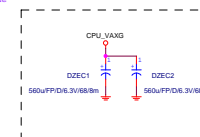
FUNCTION	MODE	SRM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubles
0	0	Tri-Seate	DUAL
1	0	Tri-Seate	Doubles
OPEN	0	Tri-Seate	Quad
open	0	open	open

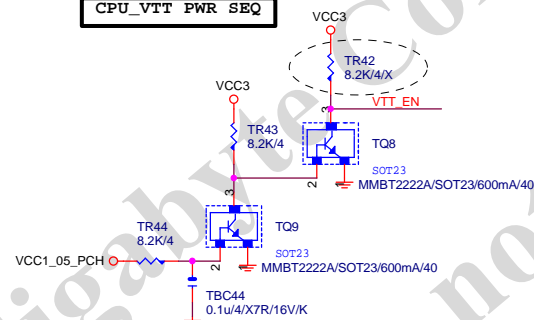
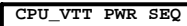
In Quad mode , IC1 pin10 link to IC2 pin

For Doubler mode

Function

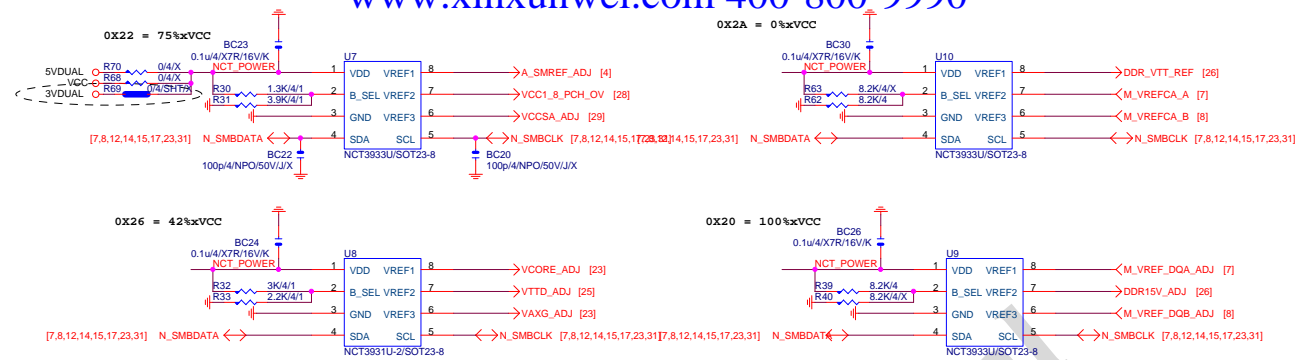
For Dual mode





	VTT_SEL
HI	1.05V
LO	1.0V

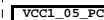
According intel
CDI/IBP#476733, 固定1.05V



NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

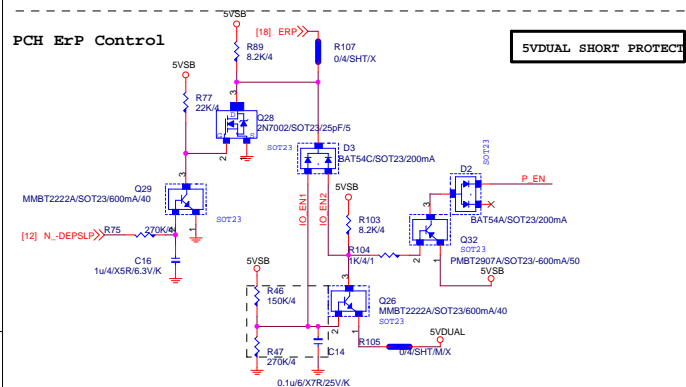
Gigabyte Technology

Title			CPU CORE VR-2
Size	Document Number	GA-Z77-D3H	
Custom		Rev	1.0
Date:	Monday, January 09, 2012	Sheet	27 of 38

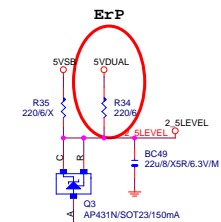


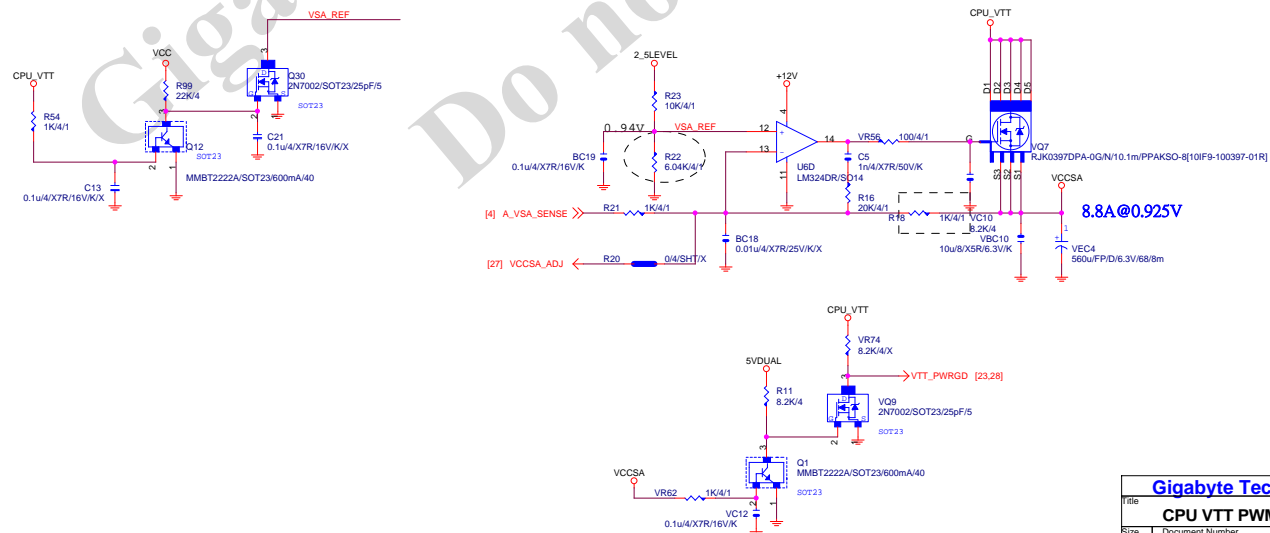
Title			
DISCRETE POWER			
Size C	Document Number	GA-Z77-D3H	Rev 1.0
Date:	Monday, January 09, 2012	Sheet	28 of 38

PCH ErP Control

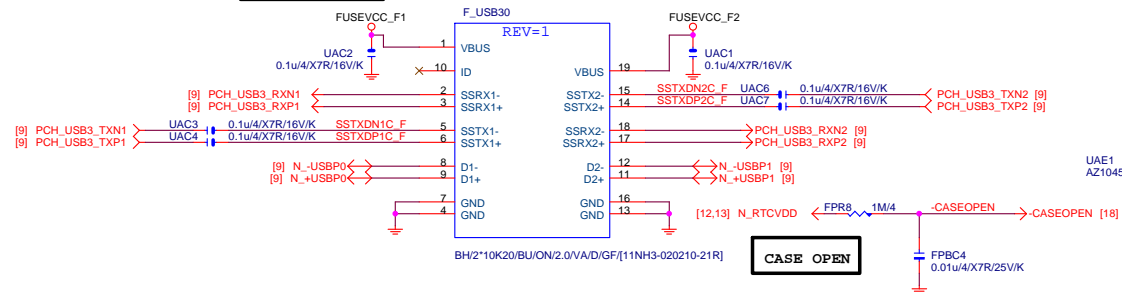


5VDUAL SHORT PROTECT

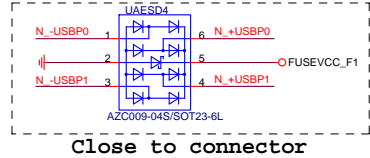




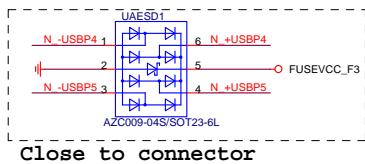
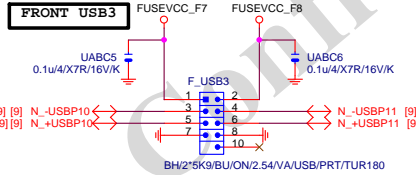
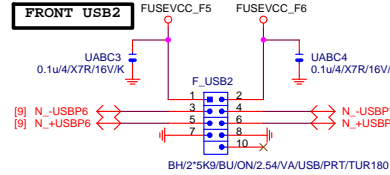
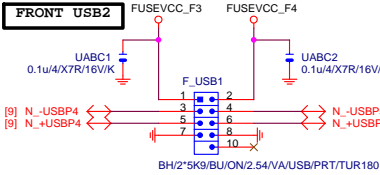
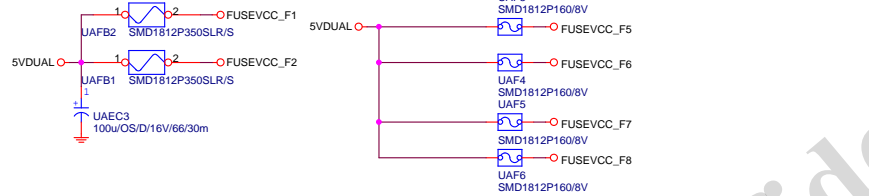
Front USB3.0



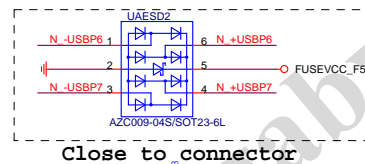
BLUE



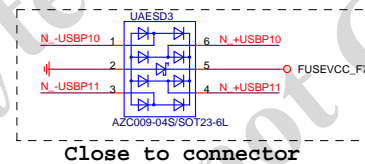
Close to connector



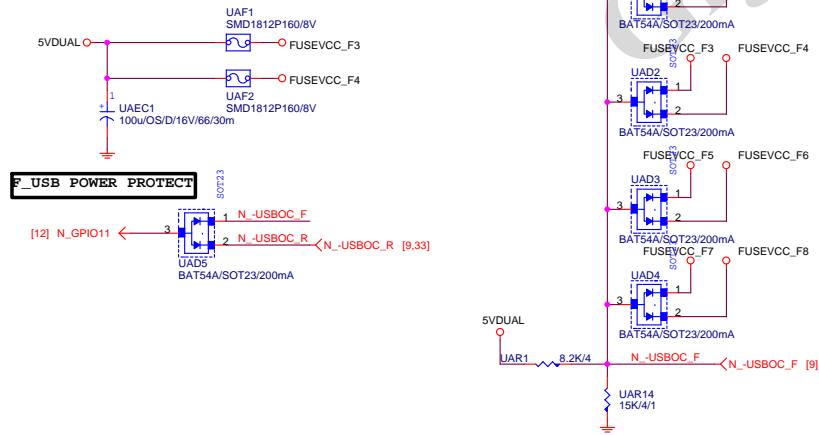
Close to connector



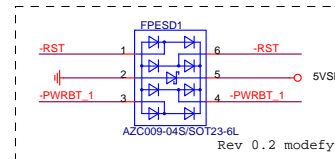
Close to connector



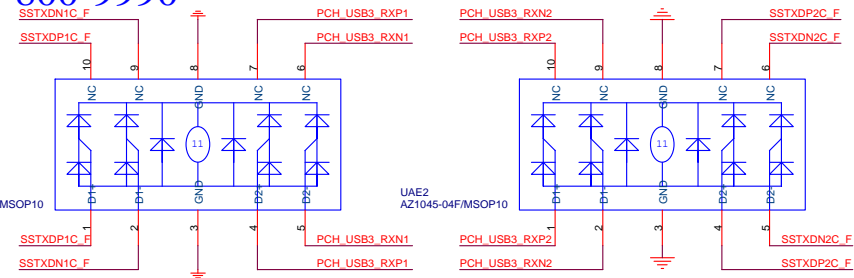
Close to connector



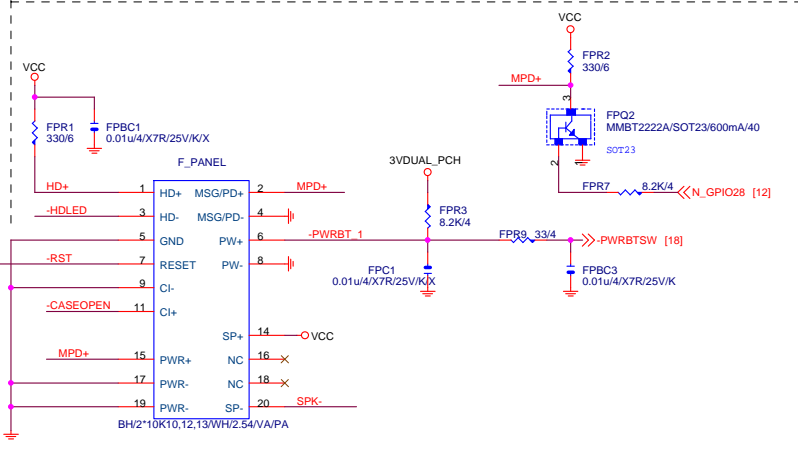
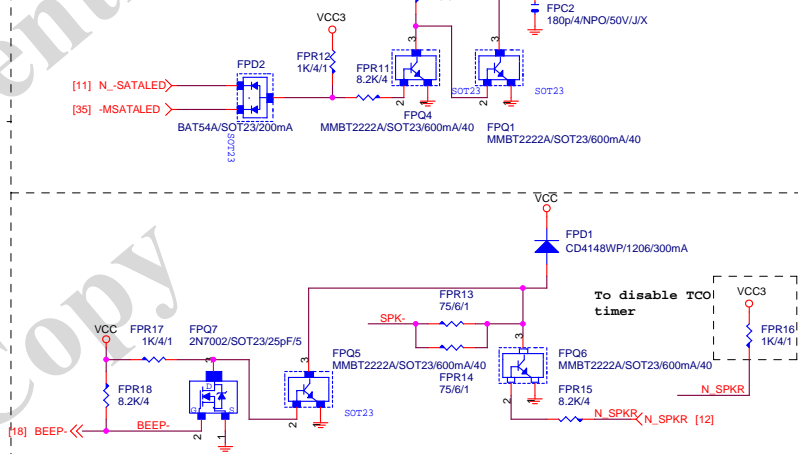
INTEL FRONT PANEL



Rev 0.2 modify



SATA LED

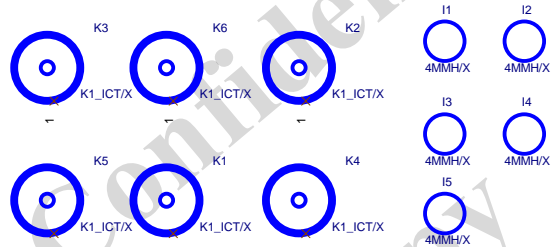
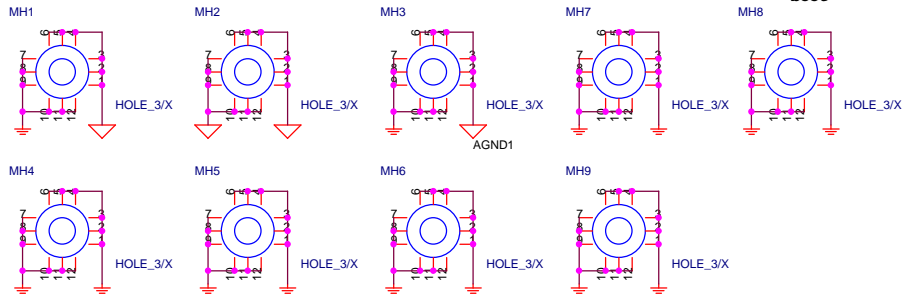
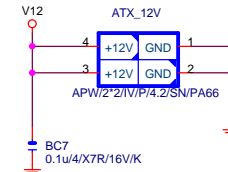
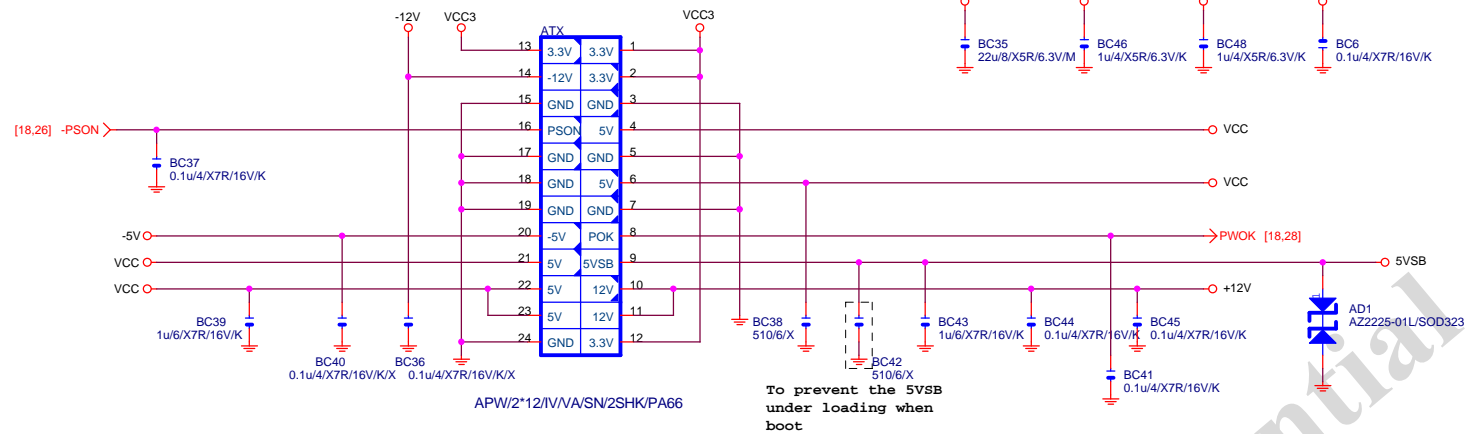


Gigabyte Technology

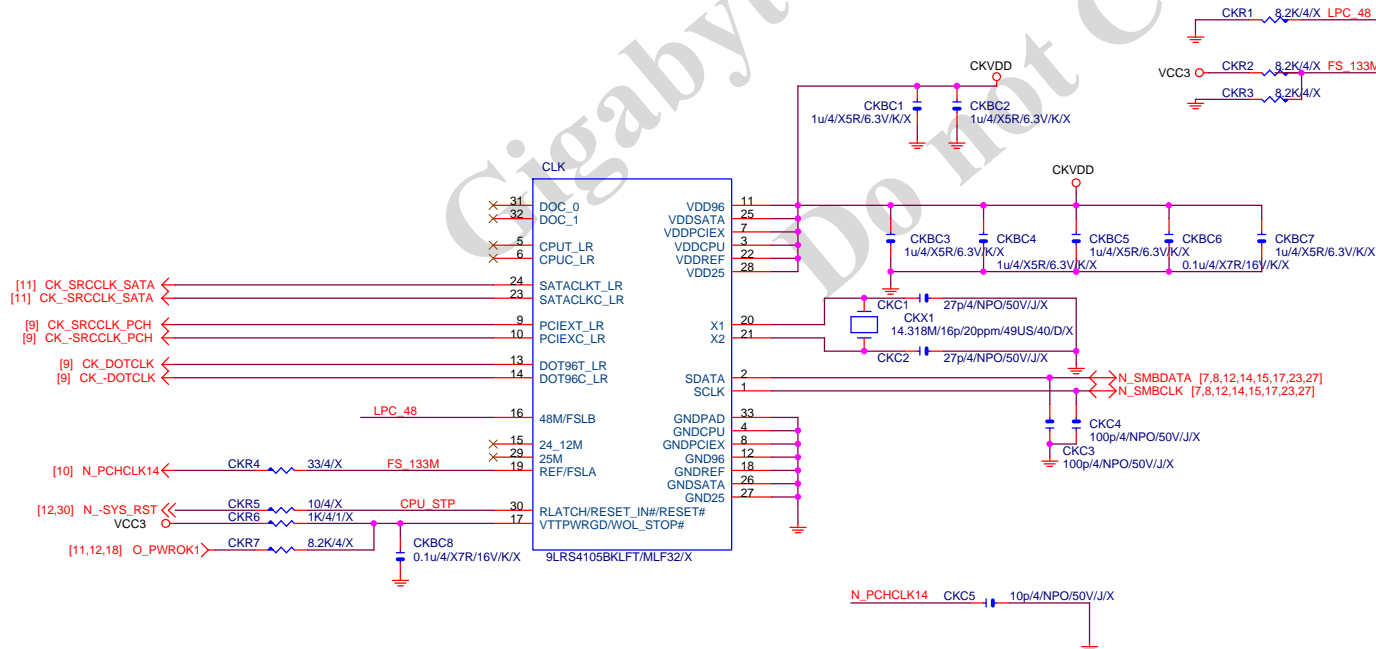
Title		FP,F_USB,USB PWR,FDD,BZ	
Size		GA-Z77-D3H	
Date		Monday, January 09, 2012	
Sheet		30 of 38	

ATX POWER CONNECTOR

www.xinxunwei.com 400-800-9990

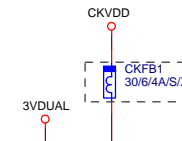


CLK GEN



CPU Frequency Selection

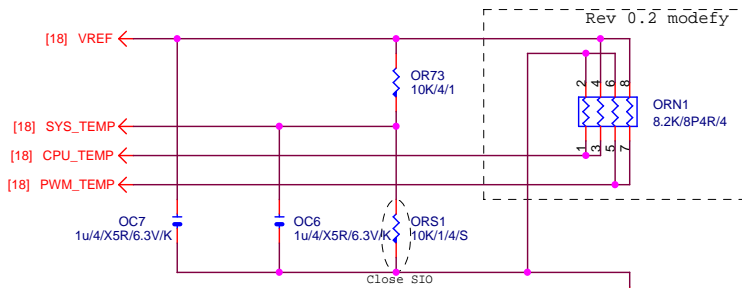
FS	CPU
0	100M <Default>
1	133M



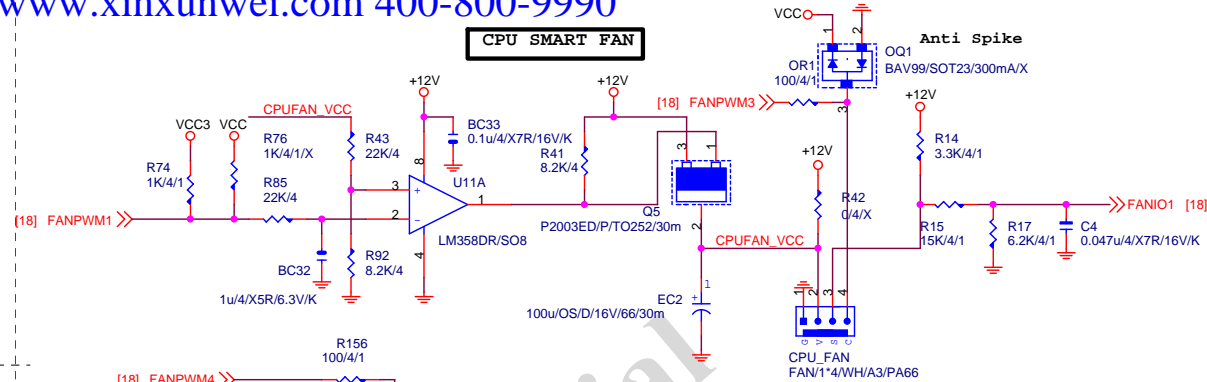
Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-Z77-D3H	1.0
Date:	Monday, January 09, 2012	Sheet 31 of 38

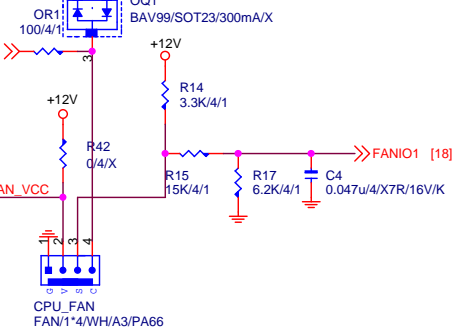
TEMP H/W MONITOR



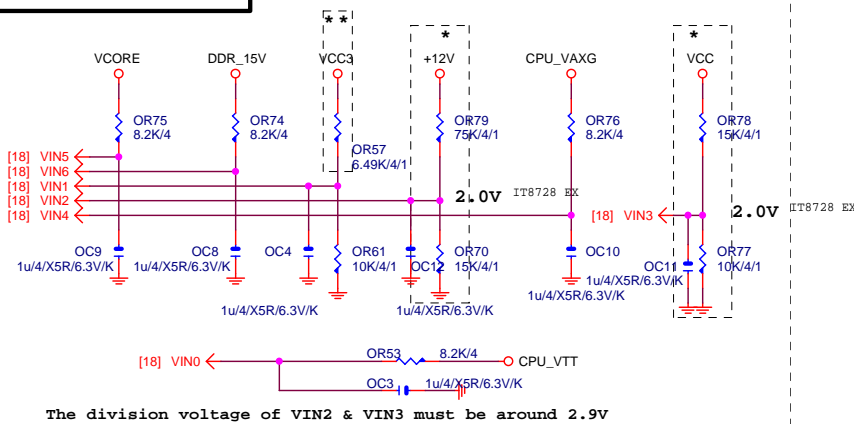
CPU SMART FAN



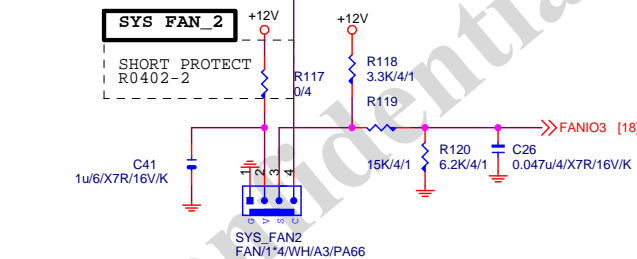
Anti Spike



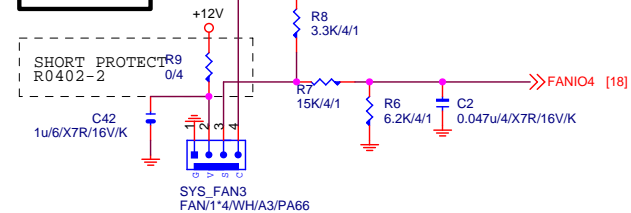
VOLTAGE-- H/W MONITOR



SYS FAN_2

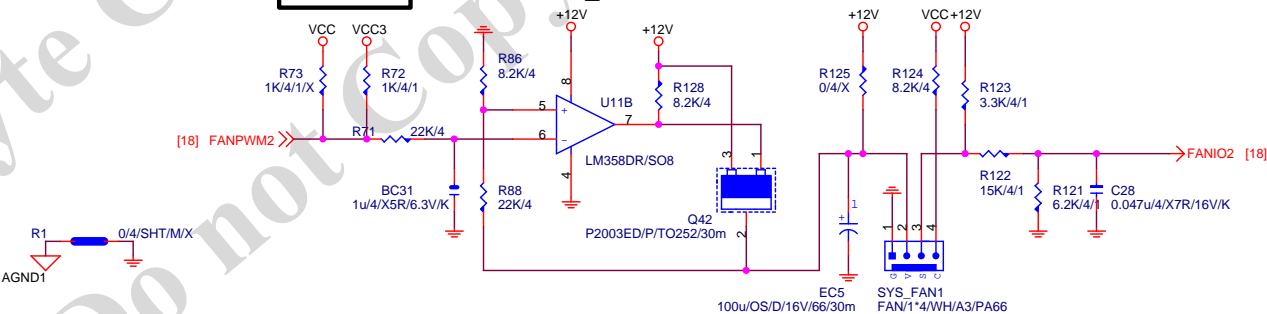


SYS FAN_3

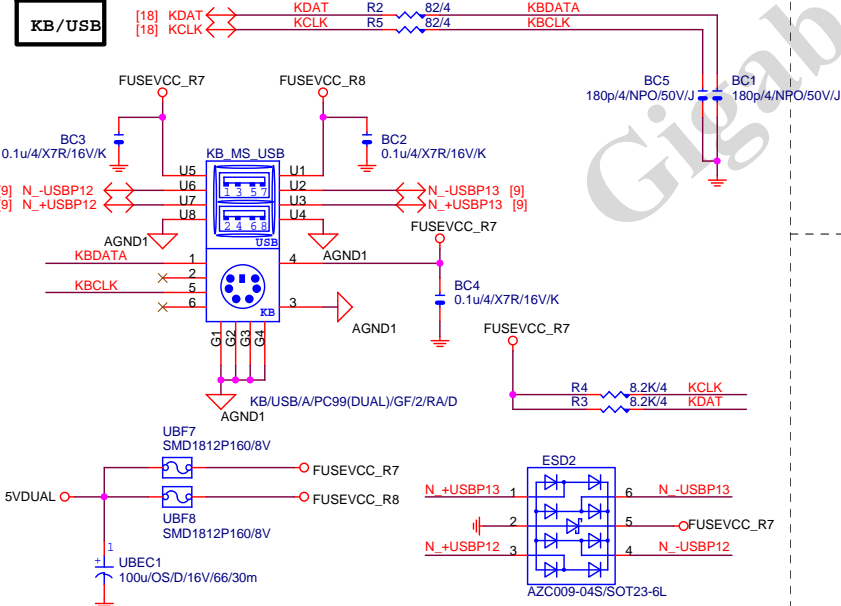


SYS FAN_1

Linear SYS_FAN



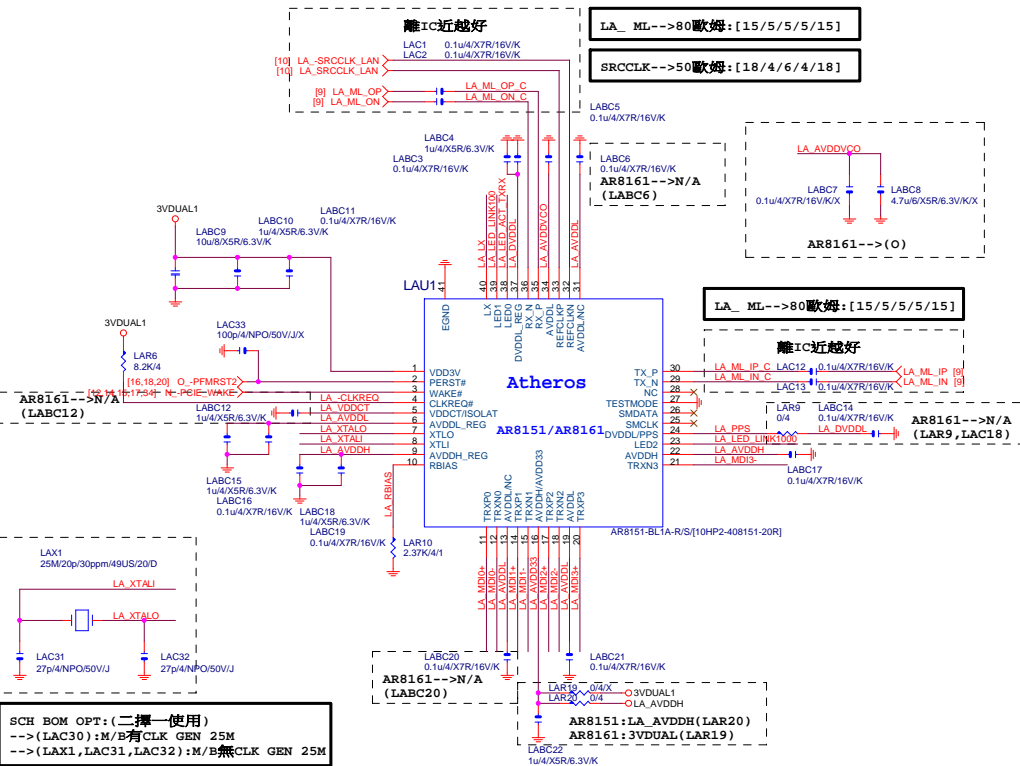
KB/USB



Gigabyte Technology

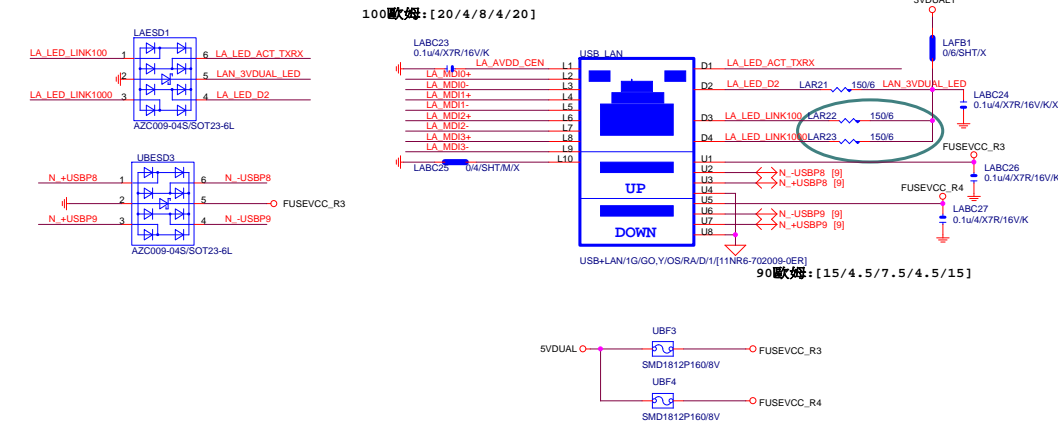
Title			HWM,KB/MS, FAN CTRL	
Size	Document Number	GA-Z77-D3H		Rev
Custom				1.0
Date:	Monday, January 09, 2012	Sheet	32 of 38	

LAN:AR8151/AR8161



SCH BOM OPT: (二擇一使用)
 -->(LAC30):M/B有CLK GEN 25M
 -->(LAX1,LAC31,LAC32):M/B無CLK GEN 25M

USB30_LAN CONNECTOR

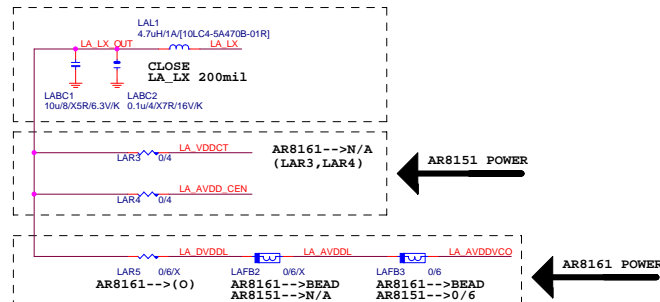


LAN POWER

NEW DESIGN ONLY FOR INTERNAL SWR

AR8151: LAR3(O), LAR5(X)

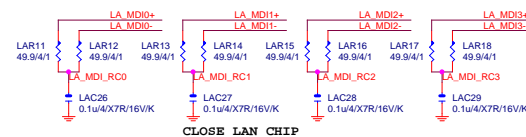
AR8161:LAR5(O),LAR3/LAR4(X)

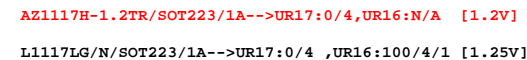
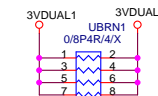
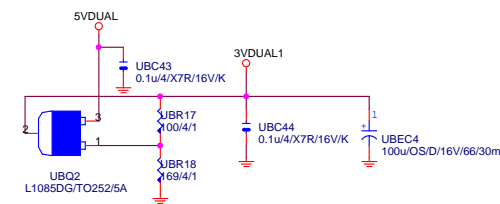



Power domain chart

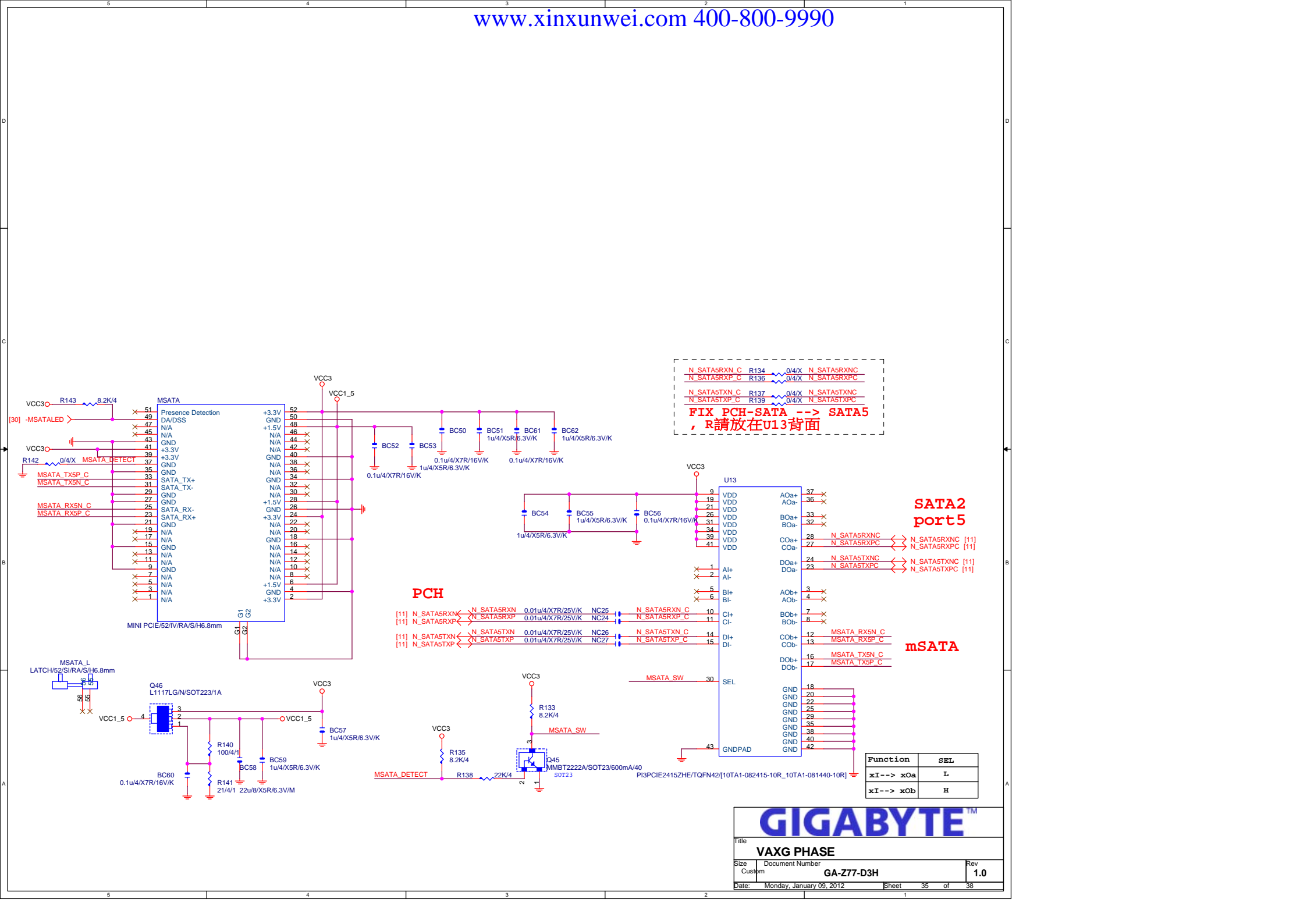
	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A





			
Title E-TRON EJ168			
Size Custom	Document Number GA-Z77-D3H		Rev 1.0
Date: Monday, January 09, 2012	Sheet	34	of 38



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FIX PCH-SATA --> SATA5
R請放在U13背面

SATA2 port5

mSATA

Function SEL
xI--> xOa L
xI--> xOb H

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Title VAXG PHASE

Size Document Number GA-Z77-D3H Rev 1.0

Date: Monday, January 09, 2012 Sheet 35 of 38

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FIX PCH-SATA --> SATA5
， R請放在U13背面

SATA2 port5

mSATA

Function	SEL
xI--> xOa	L
xI--> xOb	H

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Title VAXG PHASE

Size Document Number GA-Z77-D3H Rev 1.0

Date: Monday, January 09, 2012 Sheet 35 of 38

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mSATA

Function	SEL
xI--> xOa	L
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Title VAXG PHASE

Size Document Number GA-Z77-D3H Rev 1.0

Date: Monday, January 09, 2012 Sheet 35 of 38

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Title: VAXG PHASE

Size: Document Number: GA-Z77-D3H

Date: Monday, January 09, 2012

Sheet: 35 of 38

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Title VAXG PHASE
Size Document Number GA-Z77-D3H Rev 1.0
Date: Monday, January 09, 2012 Sheet 35 of 38

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FIX PCH-SATA --> SATA5
R請放在U13背面

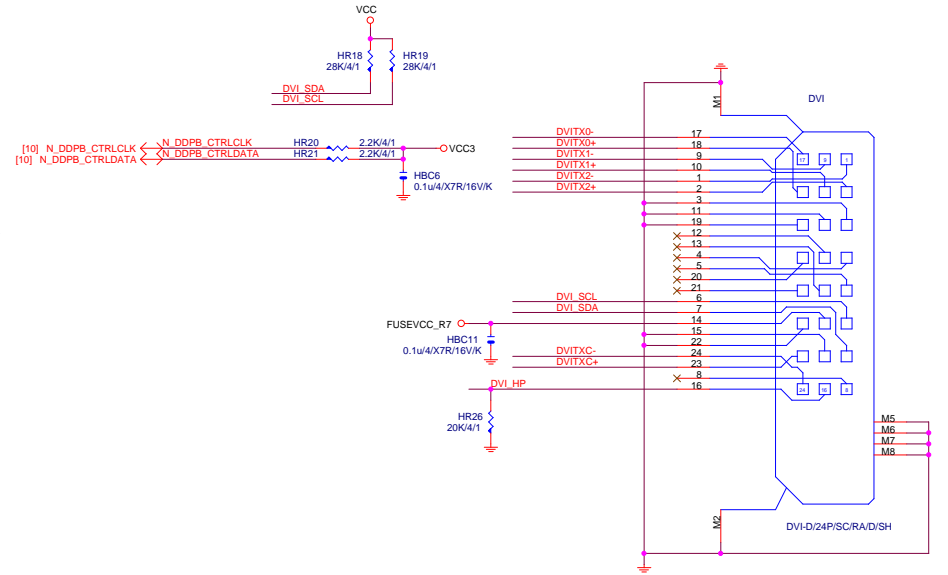
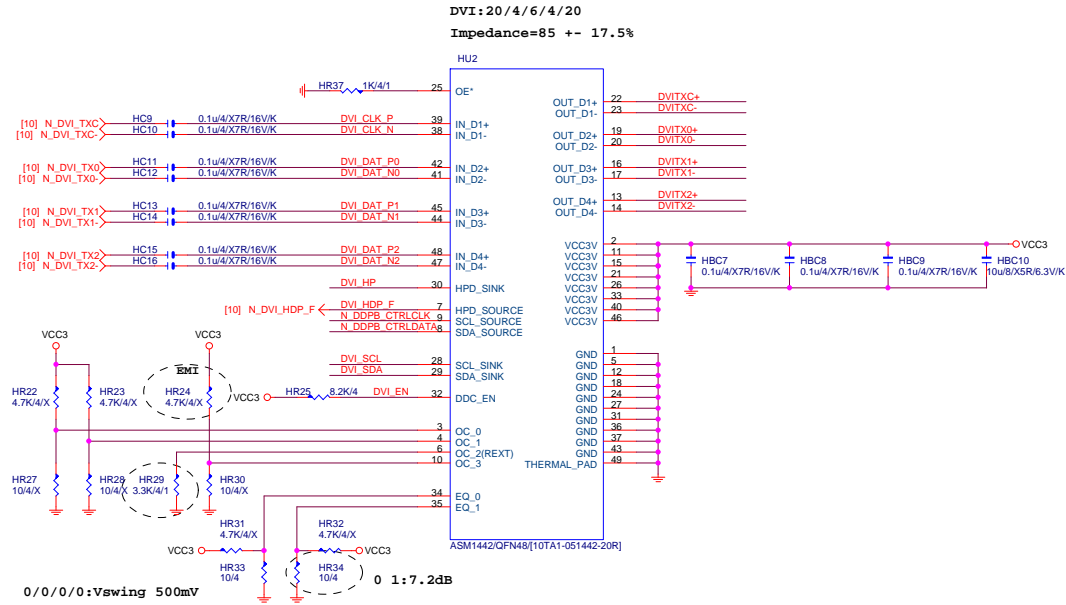
SATA2 port5

mSATA

Function SEL
xI--> xOa L
xI--> xOb H

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Title VAXG PHASE
Size Document Number GA-Z77-D3H Rev 1.0
Date: Monday, January 09, 2012 Sheet 35 of 38



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Title			TI TSB43AB23 1394	
Size			Document Number	
Custom			GA-Z77-D3H	
Date			Monday, January 09, 2012	Sheet 36 of 38

Rev
1.0

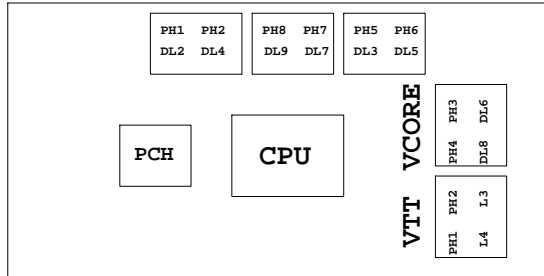
			
Title			
HDMI & USB			
Size	Document Number		Rev
Cuspm	GA-Z77-D3H		1.0
Date:	Monday, January 09, 2012	Sheet	37 of 38

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

The diagram shows the power supply architecture. On the left, the LM324 chip has several inputs: VCC3, VCC1_8_PCH, VCC3_DAC, DDR15V, and VCC1_05_PCH. Each input is connected via a resistor labeled 'L'. In the center, a voltage divider (triangle symbol) takes 5VSB and VCC as inputs and produces a 5VDUAL output. This output is fed into an ISL8014 DC-DC converter, which generates a 3VDUAL output. Finally, a second ISL8014 converter takes the 3VDUAL input to produce the final VCC1_05_MB output.

PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
Title			
TABLE LIST			
Size C	Document Number		Rev
	GA-Z77-D3H		1.0
Date:	Monday, January 09, 2012	Sheet	38 of 38